TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS039

# CD4041UB Types

## CMOS Quad True/Complement Buffer

### High Voltage Types (20-Volt Rating)

■ CD4041UB types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The CD4041UB is intended for use as a buffer, line driver, or CMOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low power dissipation are primary design requirements.

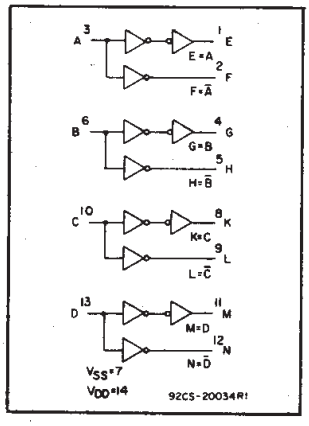
The CD4041UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

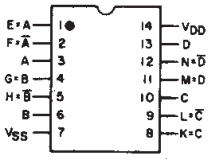
*Features:*

- Balanced sink and source current; approximately 4 times standard "B" drive
- Equalized delay to true and complement outputs
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

*Applications:*

- High current source/sink driver
- CMOS-to-DTL/TTL Converter Buffer
- Display driver
- MOS clock driver
- Resistor network driver (Ladder or weighted R)
- Buffer
- Transmission line driver




92CS-20755R1

TOP VIEW
TERMINAL ASSIGNMENT

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

**RECOMMENDED OPERATING CONDITIONS**
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | Min. | Max. | |
| Supply-Voltage Range (For $T_A$=Full Package-Temperature Range) | 3 | 18 | V |

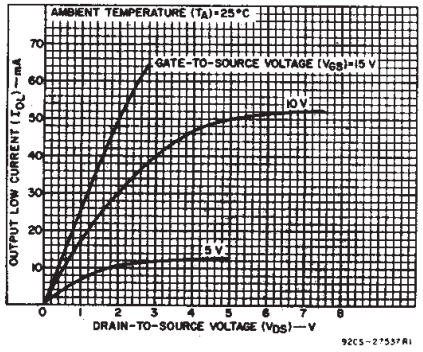



*Fig.2 – Typical output low (sink) current characteristics.*

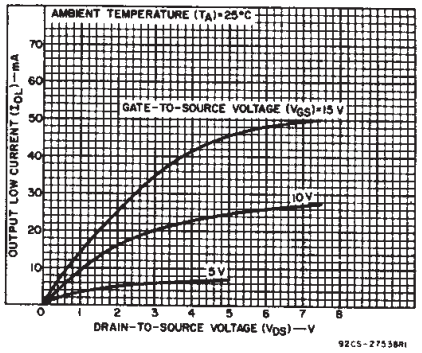



*Fig.3 – Minimum low (sink) current characteristics.*

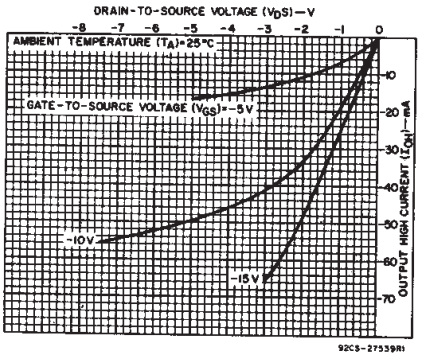



*Fig.4 – Typical output high (source) current characteristics.*

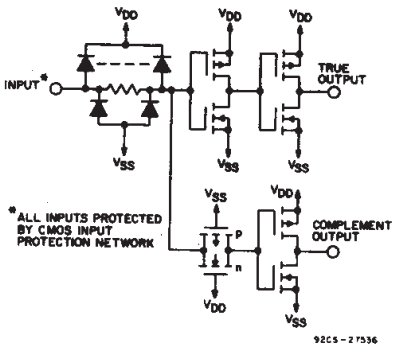



*Fig.1 – Schematic diagram 1 of 4 buffers.*

3 COMMERCIAL CMOS HIGH VOLTAGE ICs

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | +25 Min. | +25 Typ. | +25 Max. | |
| Quiescent Device Current $I_{DD}$ Max. | – | 0,5 | 5 | 1 | 1 | 30 | 30 | – | 0.02 | 1 | μA |
| | – | 0,10 | 10 | 2 | 2 | 60 | 60 | – | 0.02 | 2 | |
| | – | 0,15 | 15 | 4 | 4 | 120 | 120 | – | 0.02 | 4 | |
| | – | 0,20 | 20 | 20 | 20 | 600 | 600 | – | 0.04 | 20 | |
| Output Low (Sink) Current, $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 2.1 | 1.8 | 1.3 | 1.2 | 1.6 | 3.2 | – | mA |
| | 0.5 | 0,10 | 10 | 6.25 | 5.6 | 4 | 3.5 | 5 | 10 | – | |
| | 1.5 | 0,15 | 15 | 24 | 23 | 15.5 | 13 | 19 | 38 | – | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | −2.1 | −1.8 | -1.3 | −1.2 | −1.6 | −3.2 | – | |
| | 2.5 | 0,5 | 5 | −8.4 | −6.7 | -5.3 | −4.6 | −6.4 | −12.8 | – | |
| | 9.5 | 0,10 | 10 | −6.25 | −5.6 | -4 | −3.5 | −5 | −10 | – | |
| | 13.5 | 0,15 | 15 | −24 | −23 | -15.5 | −13 | −19 | −38 | – | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | – | 0,5 | 5 | 0.05 | | | | – | 0 | 0.05 | V |
| | – | 0,10 | 10 | 0.05 | | | | – | 0 | 0.05 | |
| | – | 0,15 | 15 | 0.05 | | | | – | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | – | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | – | |
| | – | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | – | |
| | – | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | – | |
| Input Low Voltage, $V_{IL}$ Max. | 0.5,4.5 | – | 5 | 1 | | | | – | – | 1 | V |
| | 1,9 | – | 10 | 2 | | | | – | – | 2 | |
| | 1.5,13.5 | – | 15 | 2.5 | | | | – | – | 2.5 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5,4.5 | – | 5 | 4 | | | | 4 | – | – | |
| | 1,9 | – | 10 | 8 | | | | 8 | – | – | |
| | 1.5,13.5 | – | 15 | 12.5 | | | | 12.5 | – | – | |
| Input Current, $I_{IN}$ Max. | – | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | – | $\pm 10^{-5}$ | ±0.1 | μA |

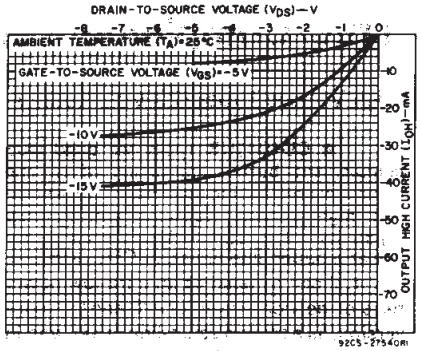



*Fig.5 – Minimum output high (source) current characteristics.*

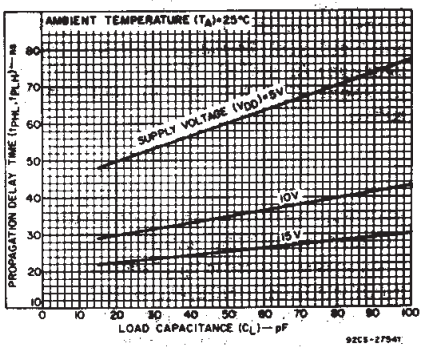



*Fig.6 – Typical propagation delay time vs. load capacitance.*

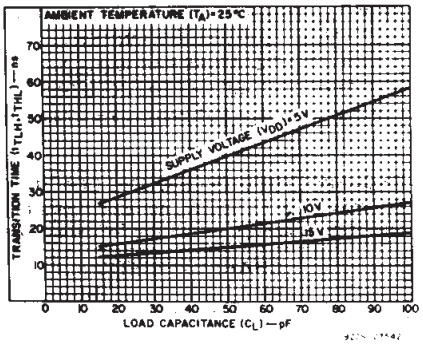



*Fig.7 – Typical transition time vs. load capacitance.*

## DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A$ = 25°C, Input $t_r$, $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200 kΩ

| CHARACTERISTIC | | CONDITIONS | LIMITS | | UNITS |
|---|---|---|---|---|---|
| | | $V_{DD}$ Volts | Typ. | Max. | |
| Propagation Delay Time: | $t_{PHL}$, $t_{PLH}$ | 5 | 60 | 120 | ns |
| | | 10 | 35 | 70 | |
| | | 15 | 25 | 50 | |
| Transition Time | $t_{THL}$, $t_{TLH}$ | 5 | 40 | 80 | ns |
| | | 10 | 20 | 40 | |
| | | 15 | 15 | 30 | |
| Input Capacitance | $C_{IN}$ | Any Input | 15 | 22.5 | pF |

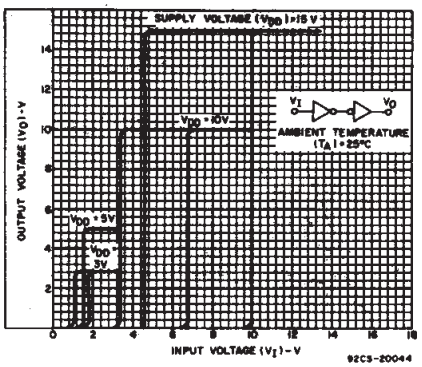



*Fig.8 – Minimum and maximum transfer characteristics – true output.*

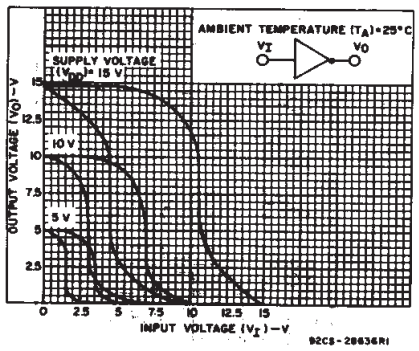



*Fig.9 — Minimum and maximum transfer characteristics — complement output.*

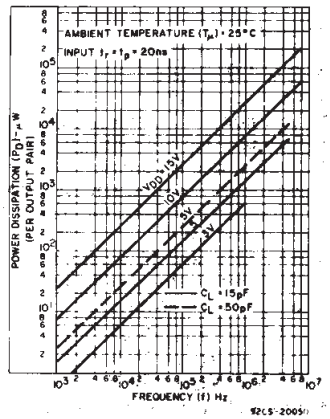



*Fig.11 — Typical power dissipation vs frequency per output pair.*

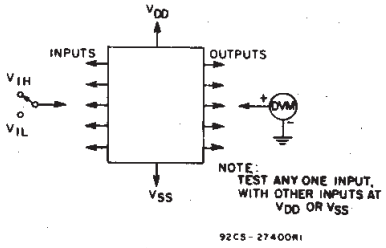



*Fig.13 — Input voltage test circuit.*

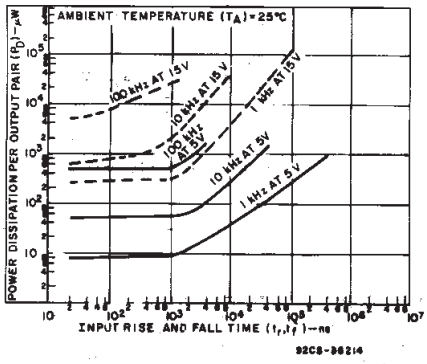



*Fig.10 — Typical power dissipation vs. input rise & fall time per output pair.*

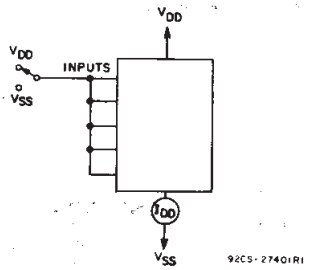



*Fig.12 — Quiescent device current test circuit.*

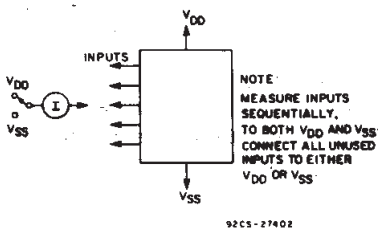
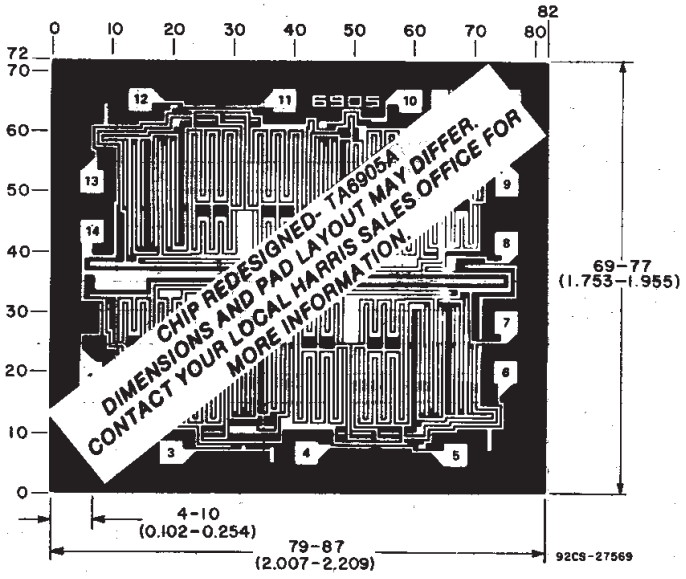



*Fig.14 — Input-leakage-current test circuit.*



**Dimensions and pad layout for the CD4041UBH**




*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated Grid graduations are in mils ($10^{-3}$ inch).*

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.