

CD4555B, CD4556B Types

CMOS Dual Binary to 1 of 4 Decoder/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4555B: Outputs High on Select

CD4556B: Outputs Low on Select

■ CD4555B and CD4556B are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input (\bar{E}), and four mutually exclusive outputs. On the CD4555B the outputs are high on select; on the CD4556B the outputs are low on select.

When the Enable input is high, the outputs of the CD4555B remain low and the outputs of the CD4556B remain high regardless of the state of the select inputs A and B. The CD4555B and CD4556B are similar to types MC14555 and MC14556, respectively.

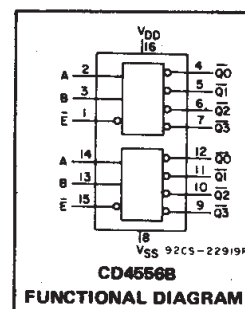
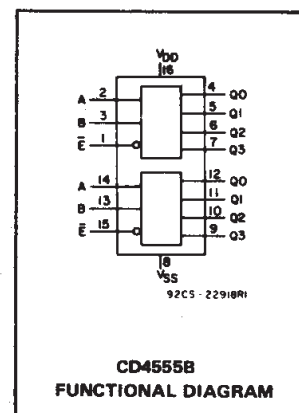
The CD4555B and CD4556B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- Expandable with multiple packages
- Standard, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Decoding
- Code conversion
- Demultiplexing (using Enable input as a data input)
- Memory chip-enable selection
- Function selection



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temp. Range)	—	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5$ V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

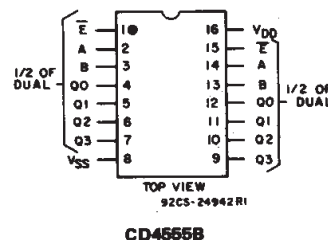
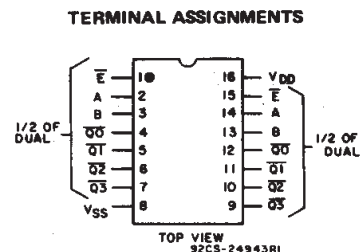
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 \pm 0.79mm) from case for 10s max $+265^\circ\text{C}$



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CD4555B, CD4556B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0,04	5	μA
	—	0,10	10	10	10	300	300	—	0,04	10	
	—	0,15	15	20	20	600	600	—	0,04	20	
	—	0,20	20	100	100	3000	3000	—	0,08	100	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	—	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	—	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	—	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	—	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	—	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	—	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0,05			—	0	0,05	—	V
	—	0,10	10	0,05			—	0	0,05	—	
	—	0,15	15	0,05			—	0	0,05	—	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4,95			4,95	5	—	—	V
	—	0,10	10	9,95			9,95	10	—	—	
	—	0,15	15	14,95			14,95	15	—	—	
Input Low Voltage, V _{IL} Max.	0,5,4,5	—	5	1,5			—	—	1,5	—	V
	1,9	—	10	3			—	—	3	—	
	1,5,13,5	—	15	4			—	—	4	—	
Input High Voltage, V _{IH} Min.	0,5,4,5	—	5	3,5			3,5	—	—	—	V
	1,9	—	10	7			7	—	—	—	
	1,5,13,5	—	15	11			11	—	—	—	
Input Current I _{IN} Max.		0,18	18	±0,1	±0,1	±1	±1	—	±10 ⁻⁵	±0,1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_p, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		V _{DD} Volts	TYP.		MAX.
Propagation Delay Time, t _{PHL} , A or B Input to t _{PLH} Any Output		5	220	440	ns
		10	95	190	
		15	70	140	
E Input to Any Output		5	200	400	ns
		10	85	170	
		15	65	130	
Transition Time t _{THL} , t _{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance C _{IN}	Any Input		5	7,5	pF

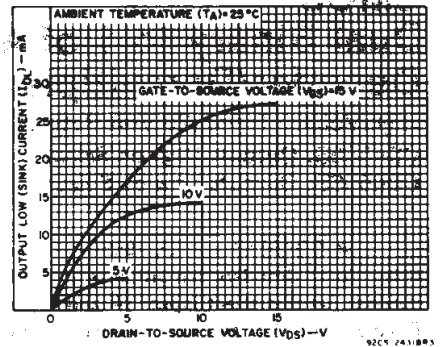


Fig. 1 — Typical output low (sink) current characteristics.

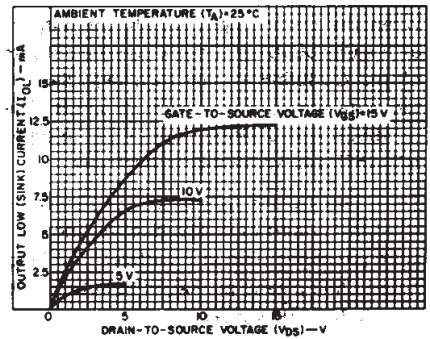


Fig. 2 — Minimum output low (sink) current characteristics.

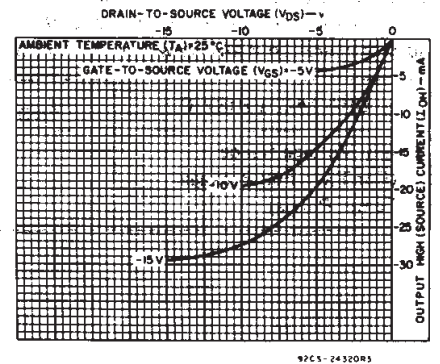


Fig. 3 — Typical output high (source) current characteristics.

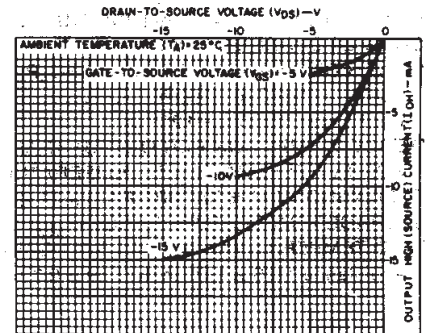


Fig. 4 — Minimum output high (source) current characteristics.

CD4555B, CD4556B Types

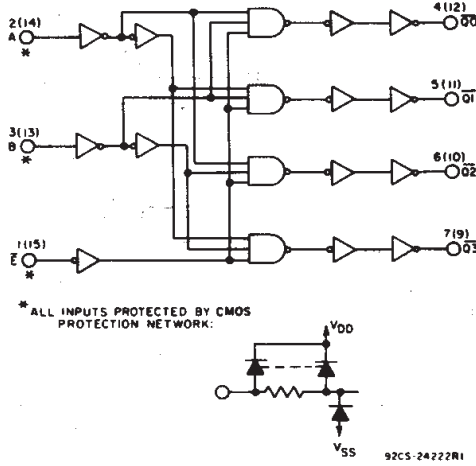


Fig. 5 - CD4556B logic diagram (1 of 2 identical circuits).

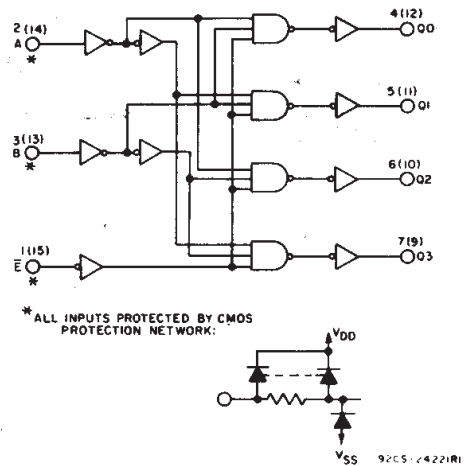


Fig. 6 - CD4555B logic diagram (1 of 2 identical circuits).

TRUTH TABLE

INPUTS			OUTPUTS CD4555B				OUTPUTS CD4556B			
\bar{E}	B	A	Q3	Q2	Q1	Q0	$\bar{Q}3$	$\bar{Q}2$	$\bar{Q}1$	$\bar{Q}0$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = DON'T CARE

LOGIC 1 \equiv HIGH
LOGIC 0 \equiv LOW

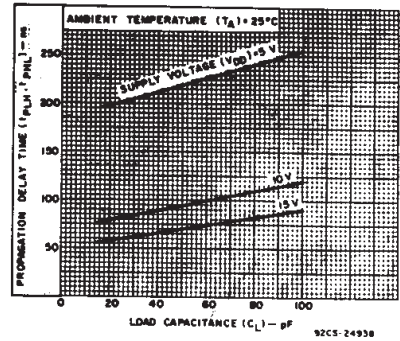


Fig. 7 - Typical propagation delay time vs. load capacitance (A or B input to any output).

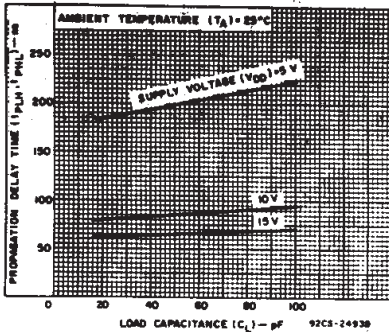


Fig. 8 - Typical propagation delay time vs. load capacitance (E input to any output).

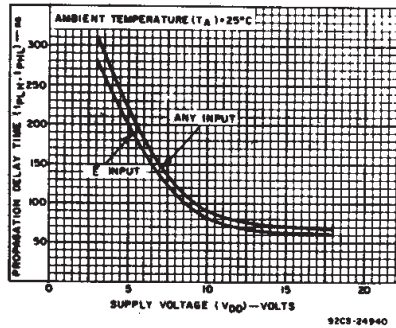


Fig. 9 - Typical propagation delay time vs. supply voltage.

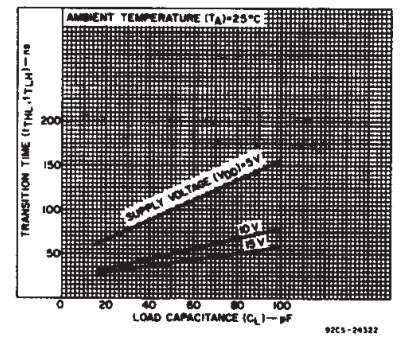


Fig. 10 - Typical transition time vs. load capacitance.

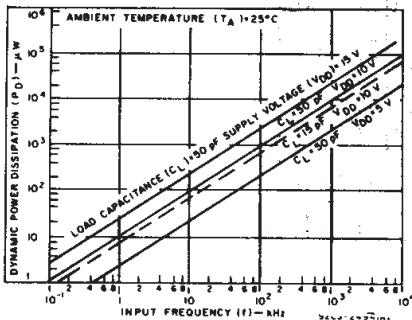


Fig. 11 - Typical dynamic power dissipation vs. frequency.

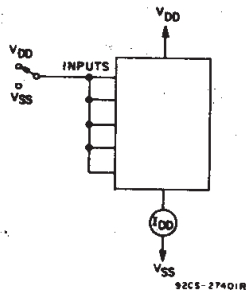


Fig. 12 - Quiescent device current test circuit.

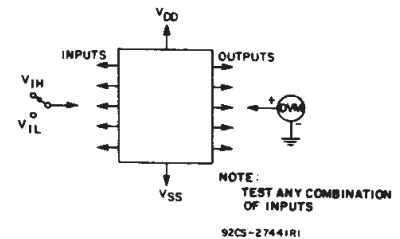


Fig. 13 - Input voltage test circuit.

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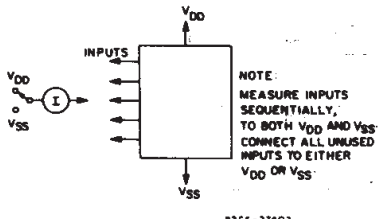


Fig. 14 - Input current test circuit.

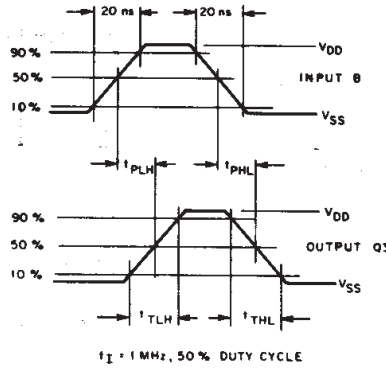


Fig. 15 - CD4555B B input to Q3 output dynamic signal waveforms.

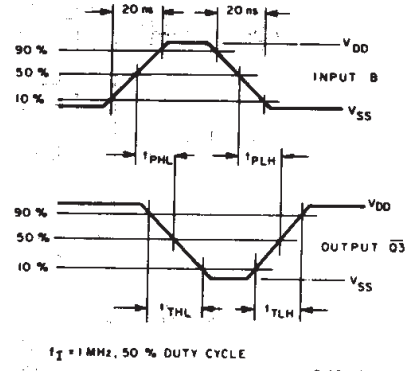


Fig. 16 - CD4556B B input to Q3 output dynamic signal waveforms.

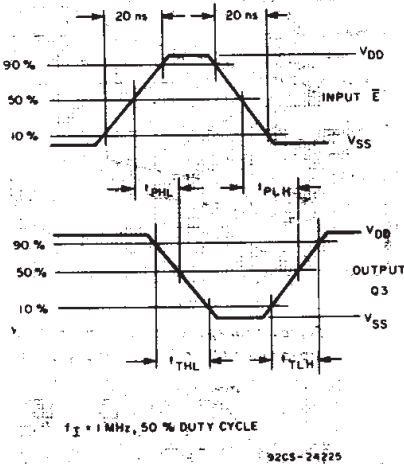


Fig. 17 - CD4555B E input to Q3 output dynamic signal waveforms.

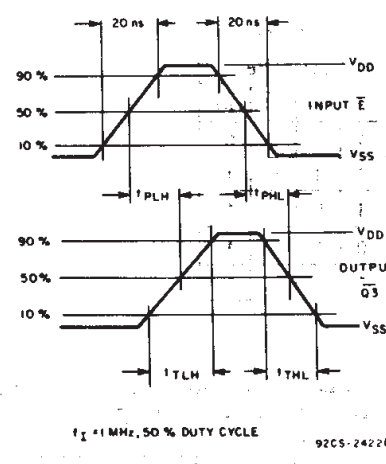
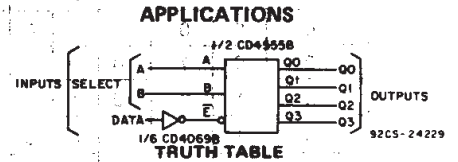


Fig. 18 - CD4556B E input to Q3 output dynamic signal waveforms.



TRUTH TABLE

SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

Fig. 19 - 1-of-4 line data demultiplexer using CD4555B.

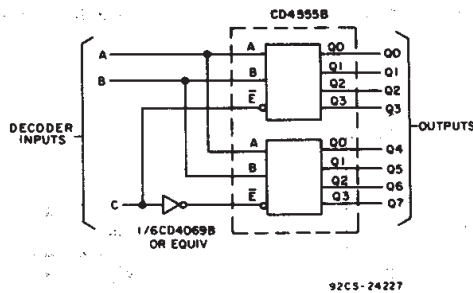


Fig. 20 - 1-of-8 decoder using CD4555B.

TRUTH TABLE

INPUTS			Q OUTPUTS							
C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

CD4555B, CD4556B Types

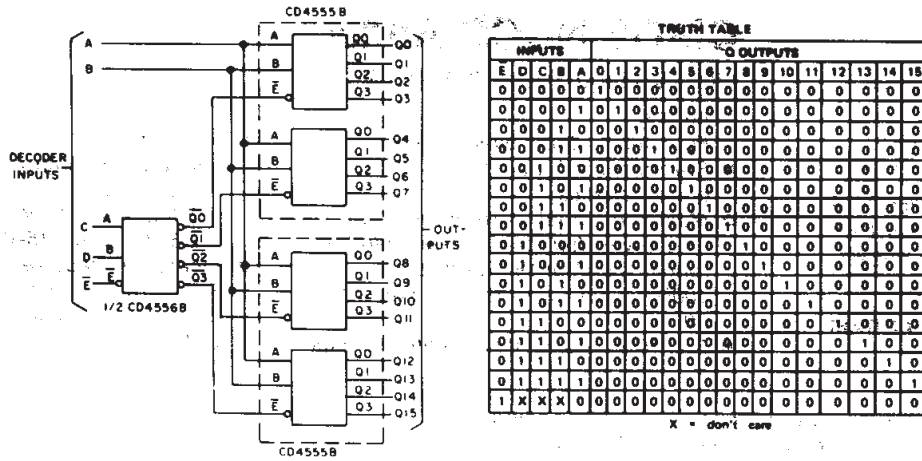
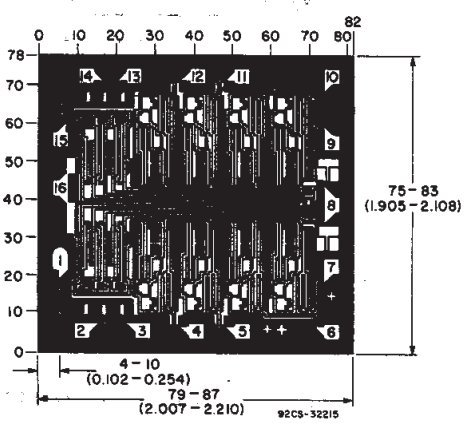
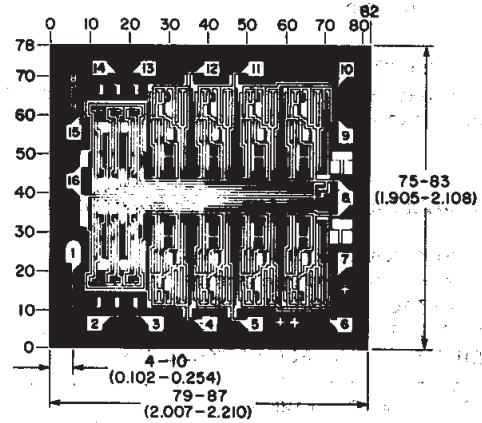


Fig. 21 - 1-of-16 decoder using CD4555B and CD4556B.



DIMENSIONS AND PAD LAYOUT FOR CD4555BH.



DIMENSIONS AND PAD LAYOUT FOR CD4556BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

COMMERCIAL CMOS HIGH VOLTAGE ICs

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