

# CD74HC75, CD74HCT75

## Dual 2-Bit Bistable Transparent Latch

### Features

- True and Complementary Outputs
- Buffered Inputs and Outputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$

at  $V_{CC} = 5V$

- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

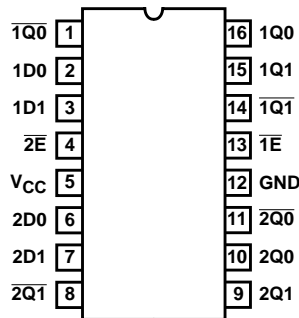
### Description

The Harris CD74HC75 and CD74HCT75 are dual 2-bit bistable transparent latches. Each one of the 2-bit latches is controlled by separate Enable inputs ( $\overline{1E}$  and  $\overline{2E}$ ) which are active LOW. When the Enable input is HIGH data enters the latch and appears at the Q output. When the Enable input ( $\overline{1E}$  and  $\overline{2E}$ ) is LOW the output is not affected.

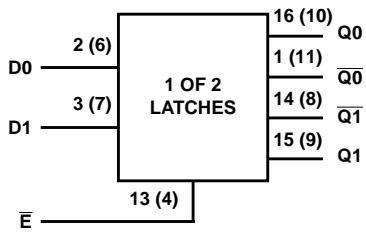
### Ordering Information

### Pinout

CD74HC75, CD74HCT75  
(PDIP, SOIC)  
TOP VIEW



**Functional Diagram**



**TRUTH TABLE**

INPUTS		OUTPUTS	
D	$\bar{E}$	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q0	$\bar{Q}0$

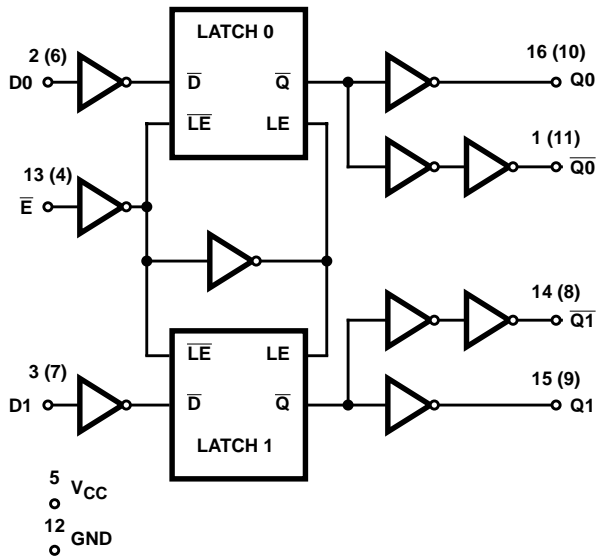
NOTE:

H = High Level

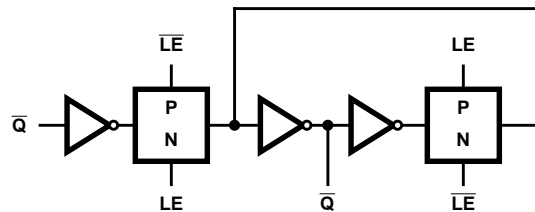
L = Low Level

X = Don't Care

Q0 = The level of Q before the transition of  $\bar{E}$ .



**FIGURE 1. LOGIC DIAGRAM**



**FIGURE 2. LATCH DETAIL**

## CD74HC75, CD74HCT75

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	90
SOIC Package .....	115
Maximum Junction Temperature (Hermetic Package or Die) . . .	$175^{\circ}C$
Maximum Junction Temperature (Plastic Package) .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$
(SOIC - Lead Tips Only)	

### Operating Conditions

Temperature Range, $T_A$ .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<b>HC TYPES</b>													
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V	
				4.5	4.4	-	-	4.4	-	4.4	-	V	
				6	5.9	-	-	5.9	-	5.9	-	V	
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V	
				-4	4.5	3.98	-	-	3.84	-	3.7	-	V
				-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V	
				4.5	-	-	0.1	-	0.1	-	0.1	V	
				6	-	-	0.1	-	0.1	-	0.1	V	
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V	
				4	4.5	-	-	0.26	-	0.33	-	0.4	V
				5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$	

## CD74HC75, CD74HCT75

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	4	-	40	-	80	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-0.02	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-4	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			0.02	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	4	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	4	-	40	-	80	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 4)	V <sub>CC</sub> - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

4. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOADS
D0, D1	0.8
1E, 2E	1.2

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

### Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<b>HC TYPES</b>												
Pulse Width Enable Input	t <sub>W</sub>	-	2	80	-	-	100	-	120	-	ns	
			4.5	16	-	-	20	-	24	-	ns	
			6	14	-	-	17	-	20	-	ns	
Setup Time D to Enable	t <sub>SU</sub>	-	2	60	-	-	75	-	90	-	ns	
			4.5	12	-	-	15	-	18	-	ns	
			6	10	-	-	13	-	15	-	ns	

## CD74HC75, CD74HCT75

### Prerequisite For Switching Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Hold Time Enable to D	t <sub>H</sub>	-	2	3	-	-	3	-	3	-	ns
			4.5	3	-	-	3	-	3	-	ns
			6	3	-	-	3	-	3	-	ns
<b>HCT TYPES</b>											
Pulse Width Enable Input	t <sub>W</sub>	-	4.5	16	-	-	20	-	24	-	ns
Setup Time D to Enable	t <sub>SU</sub>	-	4.5	12	-	-	15	-	18	-	ns
Hold Time Enable to D	t <sub>H</sub>	-	4.5	3	-	-	3	-	3	-	ns

### Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay, Data to Q	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	110	-	140	-	165	ns
		C <sub>L</sub> = 50pF	4.5	-	-	22	-	28	-	33	ns
		C <sub>L</sub> = 15pF	5	-	9	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	19	-	24	-	28	ns
Propagation Delay, Data to Q̄	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	130	-	165	-	195	ns
		C <sub>L</sub> = 50pF	4.5	-	-	26	-	33	-	39	ns
		C <sub>L</sub> = 15pF	5	-	10	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	22	-	28	-	33	ns
Propagation Delay, Enable to Q	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	130	-	165	-	195	ns
		C <sub>L</sub> = 50pF	4.5	-	-	26	-	33	-	39	ns
		C <sub>L</sub> = 15pF	5	-	10	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	22	-	28	-	33	ns
Propagation Delay, Enable to Q̄	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	130	-	165	-	195	ns
		C <sub>L</sub> = 50pF	4.5	-	-	26	-	33	-	39	ns
		C <sub>L</sub> = 15pF	5	-	11	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	22	-	28	-	33	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
		C <sub>L</sub> = 50pF	4.5	-	-	15	-	19	-	22	ns
		C <sub>L</sub> = 50pF	6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>I</sub>	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 5, 6)	C <sub>PD</sub>	-	5	-	46	-	-	-	-	pF	
<b>HCT TYPES</b>											
Propagation Delay, Data to Q	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	28	-	35	-	42	ns
		C <sub>L</sub> = 15pF	5	-	11	-	-	-	-	-	ns
Propagation Delay, Data to Q̄	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	28	-	35	-	42	ns
		C <sub>L</sub> = 15pF	5	-	11	-	-	-	-	-	ns
Propagation Delay, Enable to Q	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	28	-	35	-	42	ns
		C <sub>L</sub> = 15pF	5	-	11	-	-	-	-	-	ns

# CD74HC75, CD74HCT75

## Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay, Enable to $\bar{Q}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	30	-	38	-	45	ns
		$C_L = 15\text{pF}$	5	-	12	-	-	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	$C_I$	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 5, 6)	$C_{PD}$	-	5	-	46	-	-	-	-	-	pF

**NOTES:**

5.  $C_{PD}$  is used to determine the dynamic power consumption, per latch.
6.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## Test Circuits and Waveforms



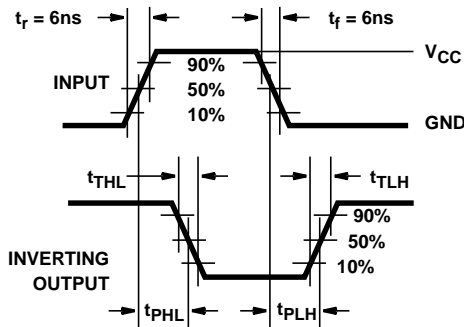
NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 3. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

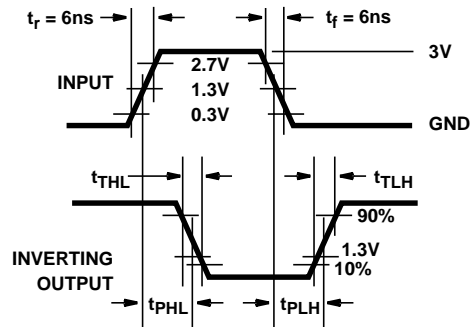


NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 4. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



**FIGURE 5. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**FIGURE 6. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

Test Circuits and Waveforms (Continued)

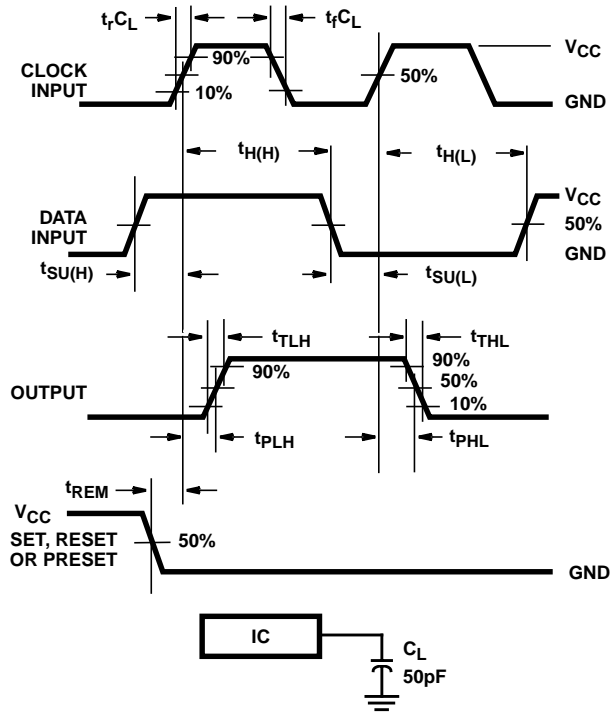


FIGURE 7. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

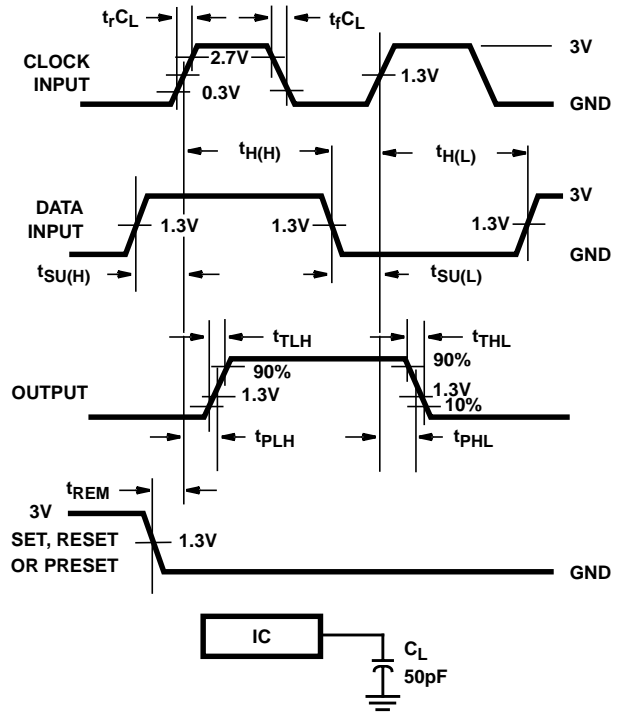


FIGURE 8. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

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