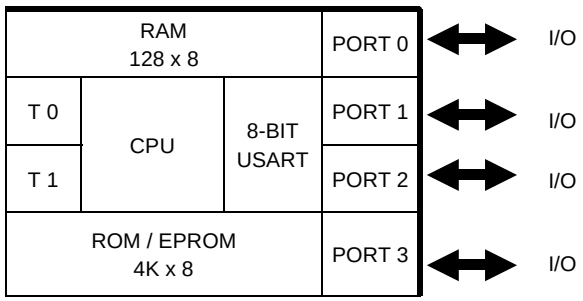
GMS90C31/51/31B/51B, GMS97C51
GMS90L31/51/31B/51B, GMS97L51 (Low voltage versions)

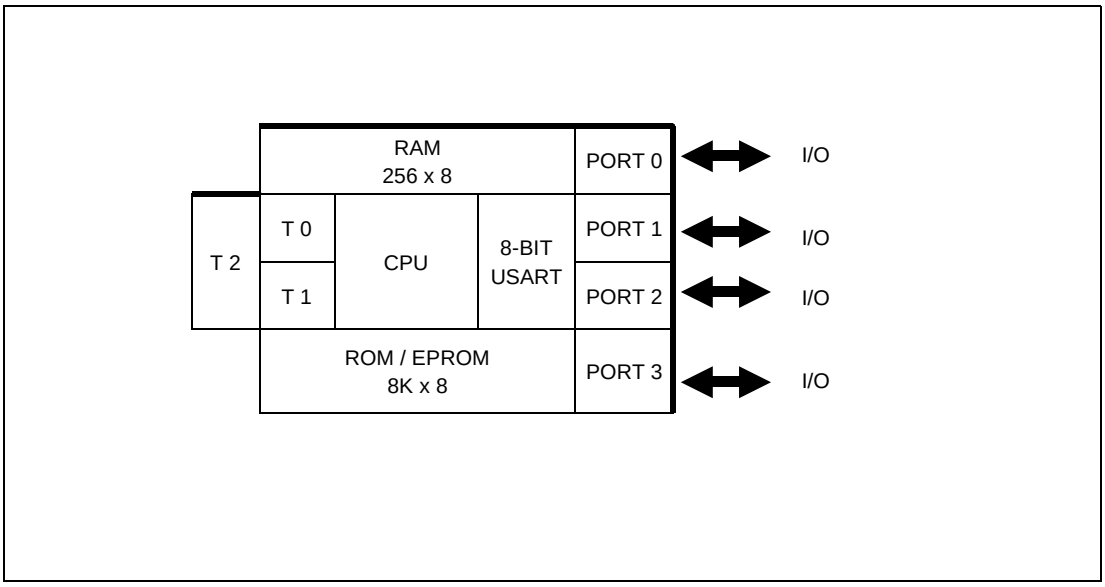
- Fully compatible to standard MCS-51 microcontroller
- Versions for 12/24/40 MHz operating frequency (90C31/51)
  Versions for 12/24/33 MHz operating frequency (90C31B/51B, 97C51)
  Low voltage versions are available 12MHz only
- 4K x 8 (EP)ROM
- 128 x 8 RAM
- 64K external program memory space
- 64K external data memory space
- Four 8-bit ports
- Two 16-bit Timers / Counters
- USART
- Five interrupt sources, two priority levels
- Power saving Idle and power down mode
- Quick pulse programming algorithm (in the OTP devices)
- 2-level program memory lock (in the OTP devices)
- 2.7Volt low voltage version available
- P-DIP-40, P-LCC-44, P-MQFP-44 package



Block Diagram

GMS90C32/52/32B/52B, GMS97C52
GMS90L32/52/32B/52B, GMS97L52 (Low voltage versions)

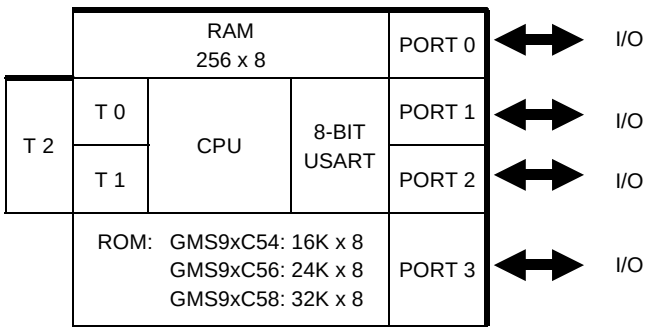
- Fully compatible to standard MCS-51 microcontroller
- Versions for 12/24/40 MHz operating frequency (90C32/52)
  Versions for 12/24/33 MHz operating frequency (90C32B/52B, 97C52)
  Low voltage versions are available 12MHz only
- 8K x 8 (EP)ROM
- 256 x 8 RAM
- 64K external program memory space
- 64K external data memory space
- Four 8-bit ports
- Three 16-bit Timers / Counters (Timer2 with up/down counter feature)
- USART
- Six interrupt sources, two priority levels
- Power saving Idle and power down mode
- Quick pulse programming algorithm (in the OTP devices)
- 2-level program memory lock (in the OTP devices)
- 2.7Volt low voltage version available
- P-DIP-40, P-LCC-44, P-MQFP-44 package



Block Diagram

GMS90C54/56/58, GMS97C54/56/58
GMS90L54/56/58, GMS97L54/56/58 (Low voltage versions)

- Fully compatible to standard MCS-51 microcontroller
- Versions for 12/24/33 MHz operating frequency
  Low voltage versions are available 12MHz only
- 16K/24K/32K bytes (EP)ROM
- 256 x 8 RAM
- 64K external program memory space
- 64K external data memory space
- Four 8-bit ports
- Three 16-bit Timers / Counters (Timer2 with up/down counter feature)
- USART
- One clock output port
- Programmable ALE pin enable / disable
- Six interrupt sources, two priority levels
- Power saving Idle and power down mode
- Quick pulse programming algorithm (in the OTP devices)
- 2-level program memory lock (in the OTP devices)
- 2.7Volt low voltage version available (with 12MHz operating frequency)
- P-DIP-40, P-LCC-44, P-MQFP-44 package



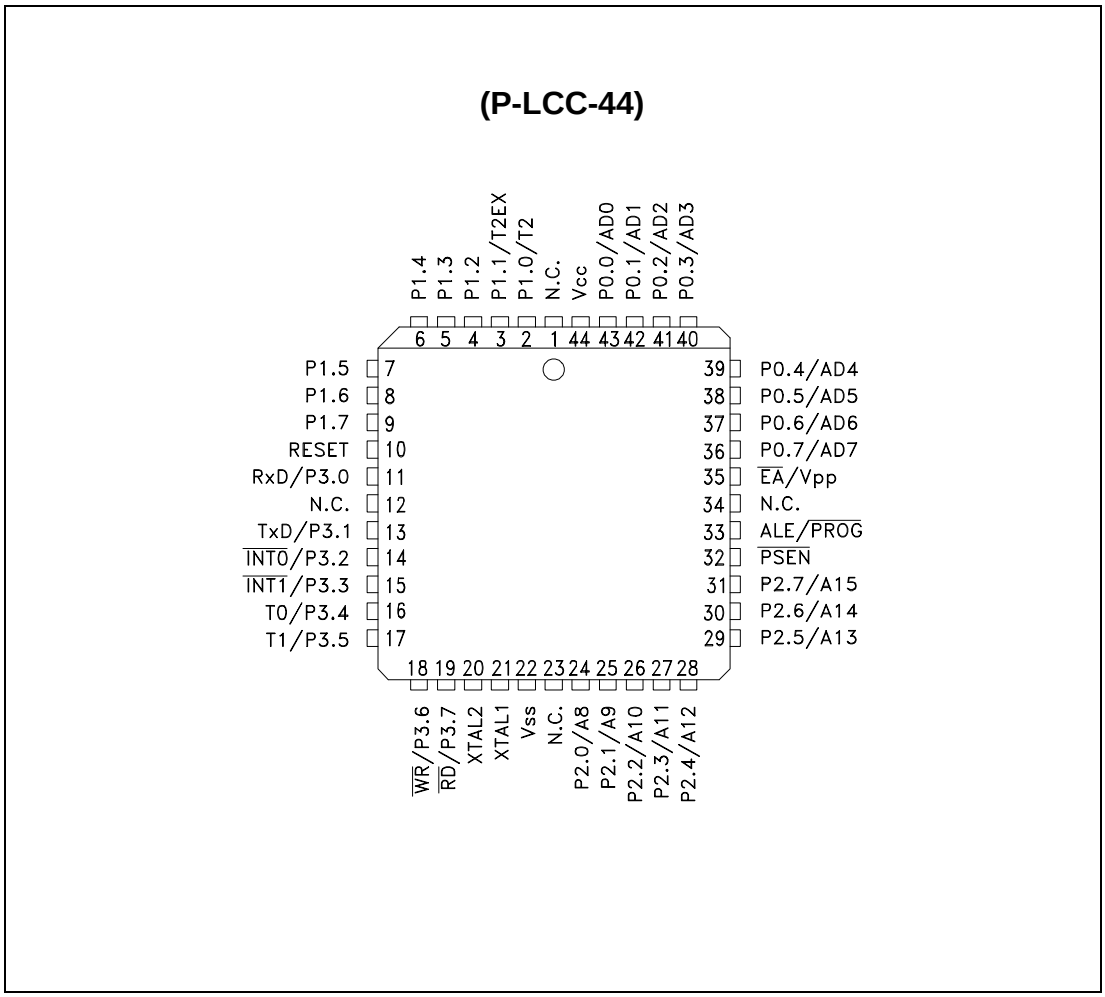
Block Diagram

GMS90 series Selection Guide

Operating voltage (V)	(EP)ROM (bytes)	RAM (bytes)	Device	Frequency (MHz)
4.25~5.5	ROM-less	128 128 256 256	GMS90C31 GMS90C31B GMS90C32 GMS90C32B	12/24/40 12/24/33 12/24/40 12/24/33
	4K 4K 8K 8K 16K 24K 32K	128 128 256 256 256 256 256	GMS90C51 GMS90C51B GMS90C52 GMS90C52B *GMS90C54 *GMS90C56 *GMS90C58	12/24/40 12/24/33 12/24/40 12/24/33 " " "
	4K OTP 8K OTP 16K OTP 24K OTP 32K OTP	128 256 256 256 256	GMS97C51 GMS97C52 GMS97C54 GMS97C56 GMS97C58	12/24/33 " " " "
2.7~5.5	ROM-less	128 128 256 256	GMS90L31 GMS90L31B GMS90L32 GMS90L32B	12
	4K 4K 8K 8K 16K 24K 32K	128 128 256 256 256 256 256	GMS90L51 GMS90L51B GMS90L52 GMS90L52B *GMS90L54 *GMS90L56 *GMS90L58	12
	4K OTP 8K OTP 16K OTP 24K OTP 32K OTP	128 256 256 256 256	GMS97L51 GMS97L52 GMS97L54 GMS97L56 GMS97L58	12

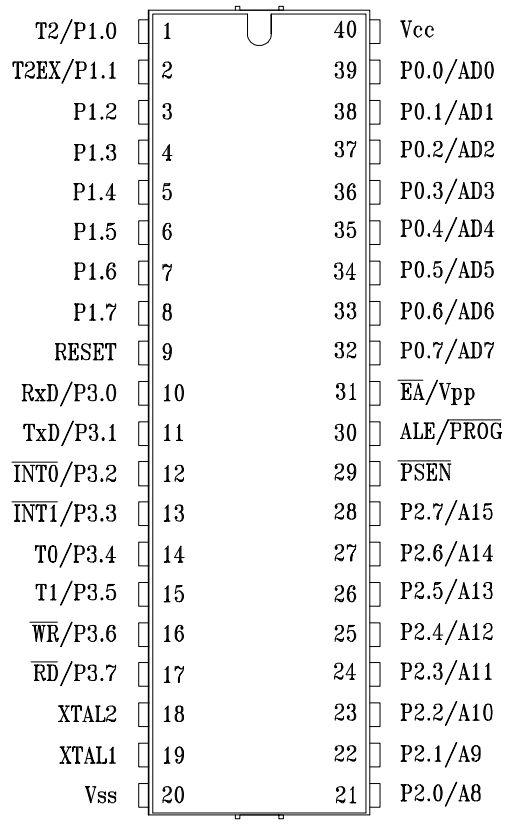
Note) * : Under development

44-PLCC Pin Configuration (top view)

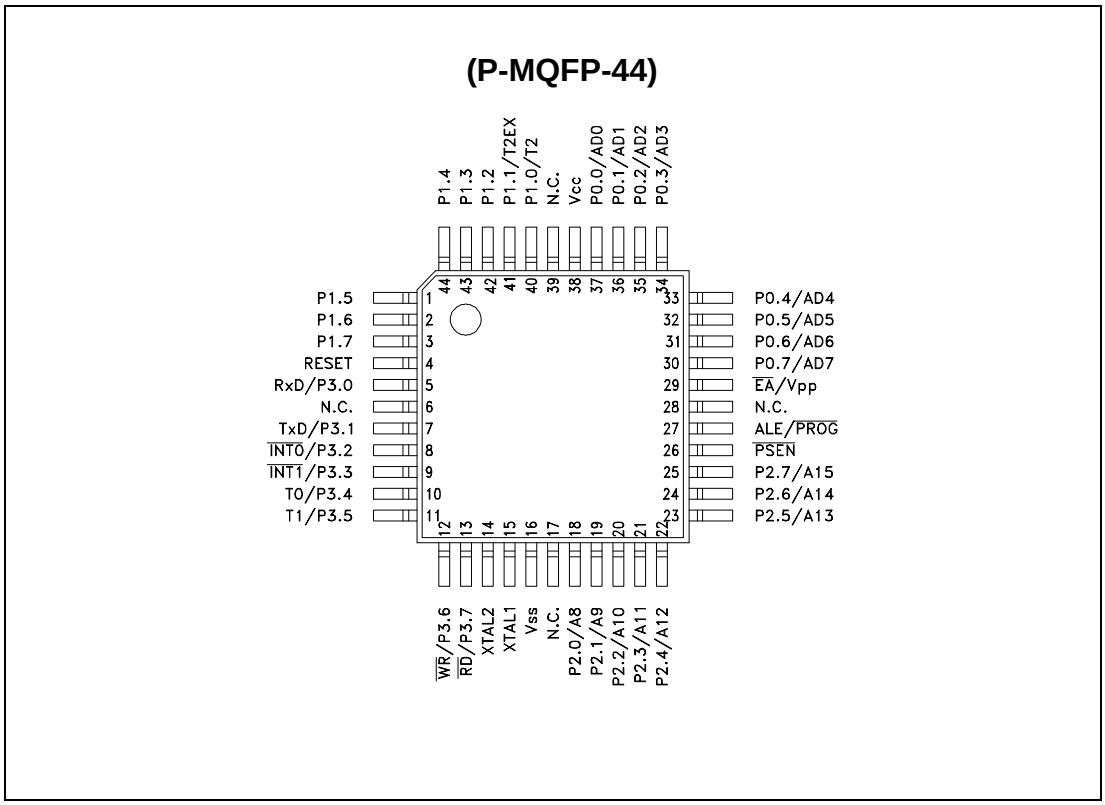


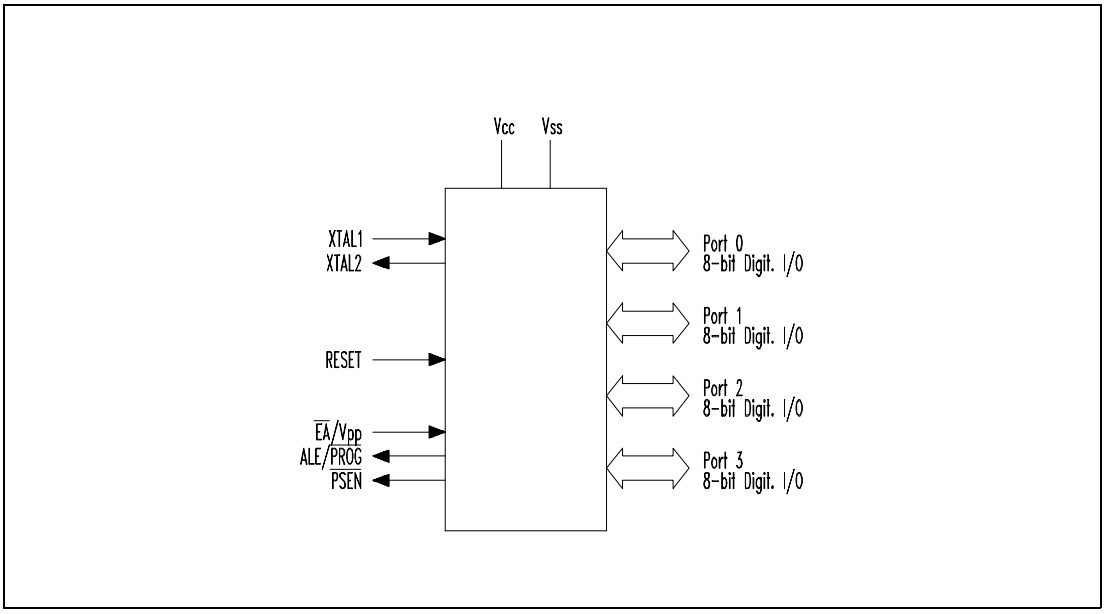
40-PDIP Pin Configuration (top view)

(P-DIP-40)



44-MQFP Pin Configuration (top view)





Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number			Input/ Output	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P1.0 - P1.7	2-9	1-8	40-44, 1-3	I/O	**Port1** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the pulls-ups (I_{IL}, in the DC characteristics). Pins P1.0 and P1.1 also. Port1 also receives the low-order address byte during program memory verification. Port1 also serves alternate functions of Timer 2.
	2	1	40		P1.0 / T2 : Timer/counter 2 external count input
	3	2	41		P1.1 / T2EX : Timer/counter 2 trigger input
					In GMS9xC54/56/58:
	2	1	40		P1.0 / T2, Clock Out : Timer/counter 2 external count input, Clock Out
P3.0 - P3.7	11, 13-19	10-17	5, 7-13	I/O	**Port 3** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 3 pins that are externally pulled low will source current because of the pulls-ups (I_{IL}, in the DC characteristics). Port 3 also serves the special features of the 80C51 family, as listed below.
	11	10	5		P3.0 / RxD receiver data input (asynchronous) or data input output(synchronous) of serial interface 0
	13	11	7		P3.1 / TxD transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0
	14	12	8		P3.2 / $\overline{INT0}$ interrupt 0 input/timer 0 gate control
	15	13	9		P3.3 / INT1 interrupt 1 input/timer 1 gate control
	16	14	10		P3.4 / T0 counter 0 input
	17	15	11		P3.5 / $\overline{T1}$ counter 1 input
	18	16	12		P3.6 / $\overline{WR}$ the write control signal latches the data byte from port 0 into the external data memory
	19	17	13		P3.7 / $\overline{RD}$ the read control signal enables the external data memory to port 0
XTAL2	20	18	14	O	**XTAL2** Output of the inverting oscillator amplifier.

Symbol	Pin Number			Input/ Output	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
XTAL1	21	19	15	I	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0 - P2.7	24-31	21-28	18-25	I/O	**Port 2** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 2 pins that are externally pulled low will source current because of the pulls-ups (I_{IL}, in the DC characteristics).Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses(MOVX @DPTR). In this application it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 special function register.
$\overline{\text{PSEN}}$	32	29	26	O	**The $\overline{\text{Program Store Enable}}$** The read strobe to external program memory when the device is executing code from the external program memory. $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
RESET	10	9	4	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.

Symbol	Pin Number			Input/ Output	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
ALE / $\overline{PROG}$	33	30	27	O	The **Address Latch Enable / $\overline{\text{Program pulse}}$** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input($\overline{PROG}$) during EPROM programming. **In GMS9xC54/56/58:** If desired, ALE operation can be disabled by setting bit 0 of SFR location $8E_H$. With this bit set, the pin is weakly pulled high. The ALE disable feature will be terminated by reset. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.
$\overline{EA}$ / V_{PP}	35	31	29	I	**$\overline{\text{External Access Enable}}$ / Program Supply Voltage** $\overline{EA}$ must be external held low to enable the device to fetch code from external program memory locations 0000_H to $FFFF_H$. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than its internal memory size. This pin also receives the 12.75V programming supply voltage(V_{PP}) during EPROM programming. Note; however, that if any of the Lock bits are programmed, EA will be internally latched on reset.
P0.0 - P0.7	43-36	39-32	37-30	I/O	**Port 0** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the GMS97C5x. External pull-up resistors are required during program verification.
V_{SS}	22	20	16	-	**Circuit ground potential**
V_{CC}	44	40	38	-	**Supply terminal** for all operating modes
N.C.	1,12, 23,34	-	6,17,28,39	-	**No connection**

Functional Description

The GMS90 series is fully compatible to the standard 8051 microcontroller family.

It is compatible with the general 8051 family. While maintaining all architectural and operational characteristics of the general 8051 family.

Figure 1 shows a block diagram of the GMS90 series

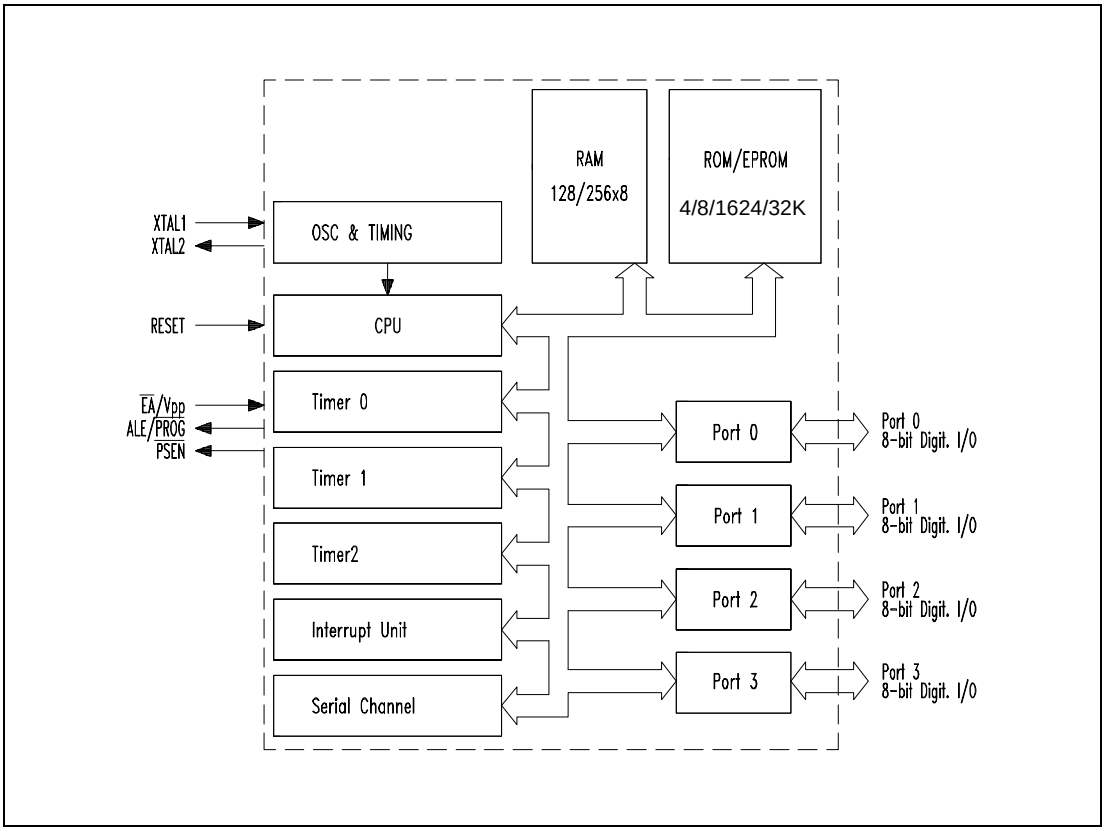


Figure 1
Block Diagram of the GMS90 series

CPU

The GMS90 series is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1.0§Á.

Special Function Register PSW

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. $D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Reset value of PSW is 00H.

Bit		Function
CY		Carry Flag
AC		Auxiliary Carry Flag (for BCD operations)
F0		General Purpose Flag
RS1 *0* *0* *1* *1*	*RS0* *0* *1* *0* *1*	Register Bank select control bits Bank 0 selected, data address 00H - 07_H Bank 1 selected, data address 08H - $0F_H$ Bank 2 selected, data address 10H - 17_H Bank 3 selected, data address 18H - $1F_H$
OV		Overflow Flag
F1		General Purpose Flag
P		Parity Flag Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 27 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in **table 1**, **table 2**, and **table 3.**

In **table 1** they are organized in numeric order of their addresses. In **table 2** they are organized in groups which refer to the functional blocks of the GMS90 series. **Table 3** illustrates the contents of the SFRs.

Table 1

Special Function Registers in Numeric Order of their Addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0**[1)]	**FF_H**	**98_H**	**SCON[1)]**	**00_H**
81_H	SP	07_H	99_H	SBUF	XX_H[2)]
82_H	DPL	00_H	$9A_H$	reserved	XX_H[2)]
83_H	DPH	00_H	$9B_H$	reserved	XX_H[2)]
84_H	reserved	XX_H[2)]	$9C_H$	reserved	XX_H[2)]
85_H	reserved	XX_H[2)]	$9D_H$	reserved	XX_H[2)]
86_H	reserved	XX_H[2)]	$9E_H$	reserved	XX_H[2)]
87_H	PCON	$0XXX000_B$[2)]	$9F_H$	reserved	XX_H[2)]
88_H	**TCON**[1)]	**00_H**	**$A0_H$**	**P2**[1)]	**FF_H**
89_H	TMOD	00_H	$A1_H$	reserved	XX_H[2)]
$8A_H$	TL0	00_H	$A2_H$	reserved	XX_H[2)]
$8B_H$	TL1	00_H	$A3_H$	reserved	XX_H[2)]
$8C_H$	TH0	00_H	$A4_H$	reserved	XX_H[2)]
$8D_H$	TH1	00_H	$A5_H$	reserved	XX_H[2)]
$8E_H$ [3)]	☞ [3)]	☞ [3)]	$A6_H$	reserved	XX_H[2)]
$8F_H$	reserved	XX_H[2)]	$A7_H$	reserved	XX_H[2)]
90_H	**P1**[1)]	**FF_H**	**$A8_H$**	**IE**[1)]	**$0X000000_B$[2)]**
91_H	reserved	00_H	$A9_H$	reserved	XX_H[2)]
92_H	reserved	XX_H[2)]	AA_H	reserved	XX_H[2)]
93_H	reserved	XX_H[2)]	AB_H	reserved	XX_H[2)]
94_H	reserved	XX_H[2)]	AC_H	reserved	XX_H[2)]
95_H	reserved	XX_H[2)]	AD_H	reserved	XX_H[2)]
96_H	reserved	XX_H[2)]	AE_H	reserved	XX_H[2)]
97_H	reserved	XX_H[2)]	AF_H	reserved	XX_H[2)]

[1)] : Bit-addressable Special Function Register.
[2)] : X means that the value is indeterminate and the location is reserved.
[3)] : The GMS9xC54/56/58 have the AUXR0 register at address $8E_H$.

GMS9xC51/52			**GMS9xC54/56/58**		
$8E_H$	reserved	XX_H [2)]	$8E_H$	AUXR0 1)	$XXXXXXX0_B$ [2)]

Special Function Registers in Numeric Order of their Addresses (continued)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$B0_H$	**P3**[1]	**FF_H**	**$D8_H$**	reserved	XX_H[2]
$B1_H$	reserved	XX_H[2]	$D9_H$	reserved	XX_H[2]
$B2_H$	reserved	XX_H[2]	DA_H	reserved	XX_H[2]
$B3_H$	reserved	XX_H[2]	DB_H	reserved	XX_H[2]
$B4_H$	reserved	XX_H[2]	DC_H	reserved	XX_H[2]
$B5_H$	reserved	XX_H[2]	DD_H	reserved	XX_H[2]
$B6_H$	reserved	XX_H[2]	DE_H	reserved	XX_H[2]
$B7_H$	reserved	XX_H[2]	DF_H	reserved	XX_H[2]
$B8_H$	**IP**[1]	**$XX000000_B$**[2]	**$E0_H$**	**ACC**[1]	**00_H**
$B9_H$	reserved	XX_H[2]	$E1_H$	reserved	XX_H[2]
BA_H	reserved	XX_H[2]	$E2_H$	reserved	XX_H[2]
BB_H	reserved	XX_H[2]	$E3_H$	reserved	XX_H[2]
BC_H	reserved	XX_H[2]	$E4_H$	reserved	XX_H[2]
BD_H	reserved	XX_H[2]	$E5_H$	reserved	XX_H[2]
BE_H	reserved	XX_H[2]	$E6_H$	reserved	XX_H[2]
BF_H	reserved	XX_H[2]	$E7_H$	reserved	XX_H[2]
$C0_H$	reserved	**XX_H[2]**	**$E8_H$**	reserved	XX_H[2]
$C1_H$	reserved	XX_H[2]	$E9_H$	reserved	XX_H[2]
$C2_H$	reserved	XX_H[2]	EA_H	reserved	XX_H[2]
$C3_H$	reserved	XX_H[2]	EB_H	reserved	XX_H[2]
$C4_H$	reserved	XX_H[2]	EC_H	reserved	XX_H[2]
$C5_H$	reserved	XX_H[2]	ED_H	reserved	XX_H[2]
$C6_H$	reserved	XX_H[2]	EE_H	reserved	XX_H[2]
$C7_H$	reserved	XX_H[2]	EF_H	reserved	XX_H[2]
$C8_H$	**T2CON**	**00_H**	**$F0_H$**	**B**[1]	**00_H**
$C9_H$[3]	T2MOD	☞ [3]	$F1_H$	reserved	XX_H[2]
CA_H	RC2L	00_H	$F2_H$	reserved	XX_H[2]
CB_H	RC2H	00_H	$F3_H$	reserved	XX_H[2]
CC_H	TL2	00_H	$F4_H$	reserved	XX_H[2]
CD_H	TH2	00_H	$F5_H$	reserved	XX_H[2]
CE_H	reserved	XX_H[2]	$F6_H$	reserved	XX_H[2]
CF_H	reserved	XX_H[2]	$F7_H$	reserved	XX_H[2]
$D0_H$	**PSW**[1]	**00_H**	**$F8_H$**	reserved	XX_H[2]
$D1_H$	reserved	XX_H[2]	$F9_H$	reserved	XX_H[2]
$D2_H$	reserved	XX_H[2]	FA_H	reserved	XX_H[2]
$D3_H$	reserved	XX_H[2]	FB_H	reserved	XX_H[2]
$D4_H$	reserved	XX_H[2]	FC_H	reserved	XX_H[2]
$D5_H$	reserved	XX_H[2]	FD_H	reserved	XX_H[2]
$D6_H$	reserved	XX_H[2]	FE_H	reserved	XX_H[2]
$D7_H$	reserved	XX_H[2]	FF_H	reserved	XX_H[2]

[1] : Bit-addressable Special Function Register
[2] : X means that the value is indeterminate and the location is reserved
[3] :

GMS9xC51/52			**GMS9xC54/56/58**		
$C9_H$	T2MOD	$XXXXXXX0_H$ [2]	$C9_H$	T2MOD	$XXXXXX00_B$ [2]

Table 2

Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$**[1)]	00_H
	B	B-Register	**$F0_H$**[1)]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word Register	**$D0_H$**[1)]	00_H
	SP	Stack Pointer	81_H	07_H
Interrupt System	IE	Interrupt Enable Register	**$A8_H$**[1)]	$0X000000_B$[2)]
	IP	Interrupt Priority Register	**$B8_H$**[1)]	$XX000000_B$[2)]
Ports	P0	Port 0	**80_H**[1)]	FF_H
	P1	Port 1	**90_H**[1)]	XX_H[3)]
	P2	Port 2	**$A0_H$**[1)]	FF_H
	P3	Port 3	**$B0_H$**[1)]	FF_H
Serial Channels	PCON[2)]	Power Control Register	87_H	$0XXX0000_B$[2)]
	SBUF	Serial Channel Buffer Reg.	99_H	XX_H[3)]
	SCON	Serial Channel 0 Control Reg.	**98_H**[1)]	00_H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	**88_H**[1)]	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Timer 2	T2CON	Timer 2 Control Register	**$C8_H$**[1)]	00_H
	T2MOD	Timer 2 Mode Register	$C9_H$	00_H
	RC2H	Timer 2 Reload Capture Reg., High Byte	CB_H	00_H
	RC2L	Timer 2 Reload Capture Reg., Low Byte	CA_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	AUXR0 [4)]	Aux. Register 0	$8E_H$	$XXXXXXX0_B$ [2)]
Power Saving Modes	PCON	Power Control Register	87_H	$0XXX0000_B$[2)]

1) Bit-addressable Special Function register
2) This special function register is listed repeatedly since some bit of it also belong to other functional blocks
3) X means that the value is indeterminate and the location is reserved
4) : The AUXR0 is in the GMS9xC54/56/58 only.

Table 3
Contents of SFR_S, SFR_S in Numeric Order

Address	Register	Bit7	6	5	4	3	2	1	0
80_H	P0								
81_H	SP								
82_H	DPL								
83_H	DPH								
87_H	PCON	SMOD	-	-	-	GF1	GF0	PDE	IDLE
88_H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89_H	TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0								
$8B_H$	TL1								
$8C_H$	TH0								
$8D_H$	TH1								
$8E_H$	AUXR0 [1]	-	-	-	-	-	-	-	A0 [1]
90_H	P1								
98_H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF								
$A0_H$	P2								
$A8_H$	IE	EA	-	ET2	ES	ET1	EX1	ET0	EX0
$B0_H$	P3								
$B8_H$	IP	-	-	PT2	PS	PT1	PX1	PT0	PX0
$C8_H$	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
$C9_H$	T2MOD	-	-	-	-	-	-	T2OE [1]	DCEN

SFR bit and byte addressable

SFR not bit addressable

- : this bit location is reserved

[1] Only in the GMS9xC54/56/58

Table 3

Contents of SFR_S, SFR_S in Numeric Order (continued)

Address	Register	Bit7	6	5	4	3	2	1	0
CA_H	RC2L								
CB_H	RC2H								
CC_H	TL2								
CD_H	TH2								
$D0_H$	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
$E0_H$	ACC								
$F0_H$	B								

SFR bit and byte addressable

SFR not bit addressable

- : this bit location is reserved

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 4:**

Table 4

Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		Gate	C/T	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{OSC}/12 \div 32$	$f_{OSC}/24 \div 32$
1	16-bit timer/counter	X	X	0	1	$f_{OSC}/12$	$f_{OSC}/24$
2	8-bit timer/counter with 8-bit autoreload	X	X	1	0	$f_{OSC}/12$	$f_{OSC}/24$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{OSC}/12$	$f_{OSC}/23$

In the "timer" function (C/$\overline{T}$ = "0") the register is incremented every machine cycle. therefore the count rate is $f_{OSC}/12$.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 2** illustrates the input clock logic.

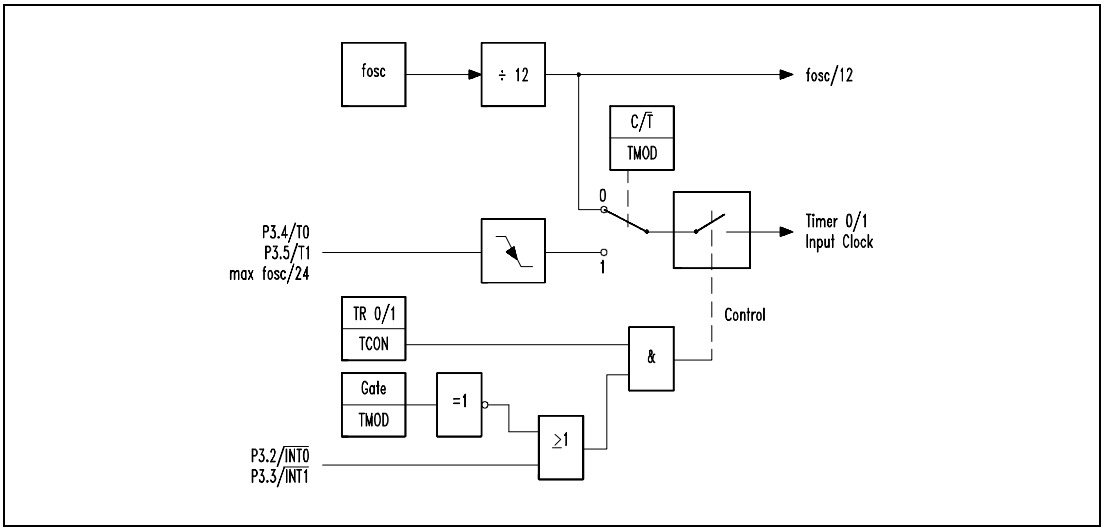


Figure 2

Timer/Counter 0 and 1 Input Clock Logic

Timer 2

Timer 2 is a 16-bit timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/$\overline{T2}$ (T2CON.1). It has three operating modes as shown in **table 5.**

Table 5

Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	RxCLK or TxCLK	CP/ RL2	TR2	DCEN	EXEN			internal	external (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	f_{OSC}/ 12	max f_{OSC}/ 24
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Capture	0	1	1	X	0	X	16 bit Timer/ Counter (only up-counting) capture TH2, TL2 to RC2H, RC2L	f_{OSC}/ 12	max f_{OSC}/ 24
	0	1	1	X	1	↓			
Baud Rate Generator	1	X	1	X	0	X	no overflow interrupt request (TF2) extra external interrupt ("Timer 2")	f_{OSC}/ 2	max f_{OSC}/ 24
	1	X	1	X	1	↓			
off	X	X	0	X	X	X	Timer 2 stops	-	-

Note : ↓ = falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 6.** The possible baud rates can be calculated using the formulas given in **table 7.**

Table 6

USART Operating Modes

Mode	SCON		Baud rate	Description
	SM0	SM1		
0	0	0	f_{OSC}/ 12	Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	f_{OSC}/ 32 or f_{OSC}/ 64	9-bit UART 11bits are transmitted (TxD) or received (RxD)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7

Formulas for Calculating Baud rates

Baud Rate derived from	Interface Mode	Baud rate
Oscillator	0 2	f_{OSC}/ 12 $(2^{SMOD} \times f_{OSC})$ / 64
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times$ timer 1 overflow rate) /32 $(2^{SMOD} \times f_{OSC})/(32 \times 12 \times (256-TH1))$
Timer2	1,3	f_{OSC} / (32 × (65536-(RC2H, RC2L)

Interrupt System

The GMS90 series provides 5 or 6 interrupt sources with two priority levels. **Figure 3** gives a general overview of the interrupt sources and illustrates the request and control flags.

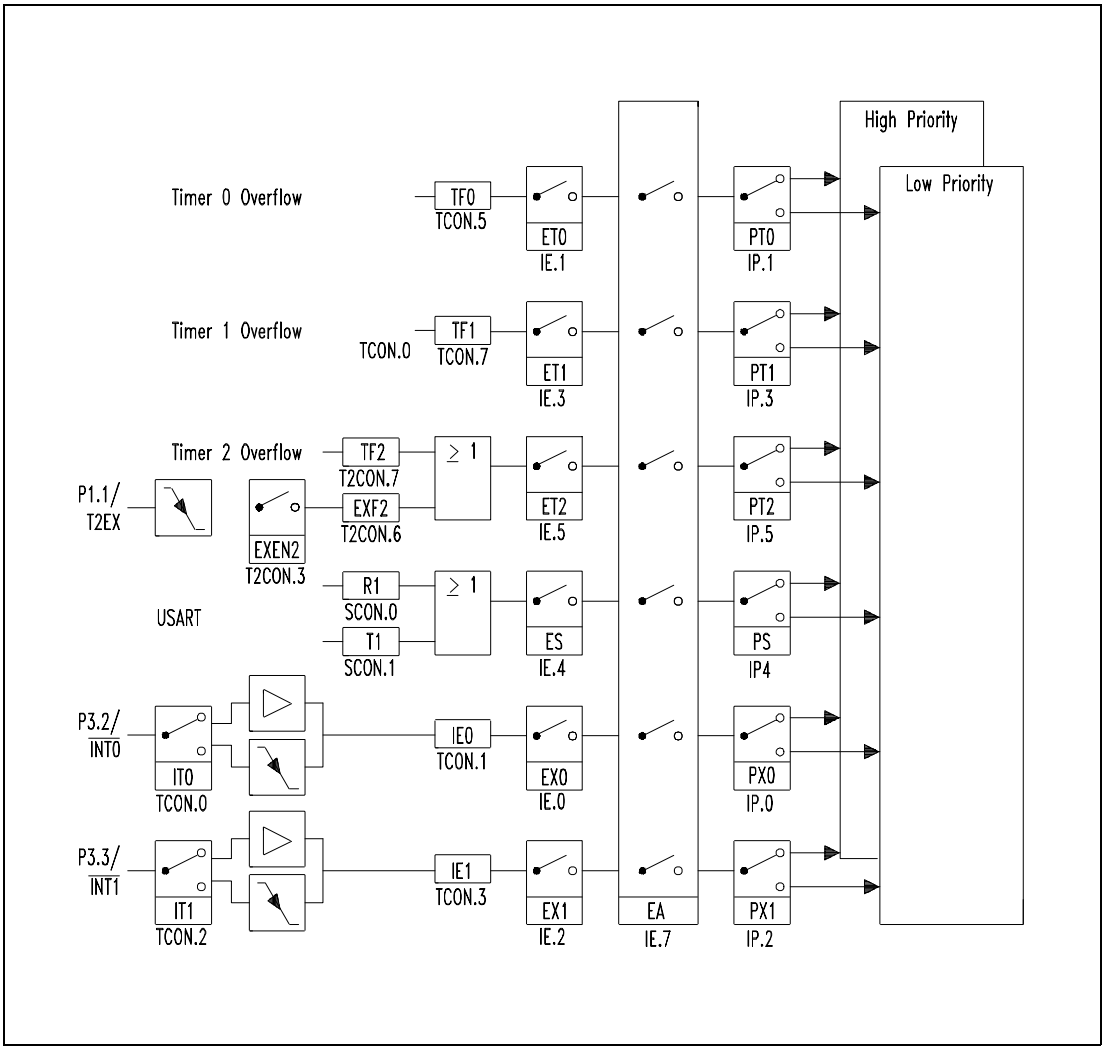


Figure 3
Interrupt Request Sources

Table 8

Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vector	Vector Address
RESET	RESET	0000_H
IE0	External interrupt 0	0003_H
TF0	Timer 0 interrupt	$000B_H$
IE1	External interrupt 1	0013_H
TF1	Timer 1 interrupt	$001B_H$
RI + TI	Serial port interrupt	0023_H
TF2 + EXF2	Timer 2 interrupt	002BH

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 9.**

Table 9

Interrupt Priority-Within-Level

Interrupt Source		Priority
External Interrupt 0	IE0	High
Timer 0 Interrupt	TF0	¡é
External Interrupt 1	IE1	¡é
Timer 1 Interrupt	TF1	¡é
Serial Channel	RI + TI	¡é
Timer 2 Interrupt	TF2 EXF2	Low

Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. **Table 10** gives a general overview of the power saving modes.

Table 10

Power Saving Modes Overview

Mode	Entering Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H	- Enabled interrupt - Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power-down Mode	ORL PCON, #02H	Hardware Reset	Oscillator is stopped, contents of on-chip RAM and SFRs are maintained (leaving Power Down Mode means redefinition of SFR contents).

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down Mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down Mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A) .....-40 to + 85¡É
Storage temperature (T_{ST}) .....-65 to + 150 ¡É

Voltage on V_{CC} pins with respect to ground (V_{SS}) .....-0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) .....-0.5 to V_{CC} + 0.5 V

Input current on any pin during overload condition .....-10 mA to + 10 mA
Absolute sum of all input currents during overload condition ..... | 100 mA |

Power dissipation .....TBD

Note : *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.*

DC Characteristics for GMS90C31/32, GMS90C51/52
GMS90C31B/32B, GMS90C51B/52B

V_{CC} = 5 V + 10%, - 15%; V_{SS} = 0 V; T_A = 0 ¡É to 70 ¡É

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except EA, RESET)	V_{IL}	-0.5	0.2 V_{CC} - 0.1	V	-
Input low voltage (EA)	$V_{IL\ 1}$	-0.5	0.2 V_{CC} - 0.3	V	-
Input low voltage (RESET)	$V_{IL\ 2}$	-0.5	0.2 V_{CC} + 0.1	V	-
Input high voltage (except XTAL1, EA, RESET)	V_{IH}	0.2V_{CC} + 0.9	V_{CC} + 0.5	V	-
Input high voltage to XTAL1	$V_{IH\ 1}$	0.7V_{CC}	V_{CC} + 0.5	V	-
Input high voltage to EA, RESET	$V_{IH\ 2}$	0.6V_{CC}	V_{CC} + 0.5	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45	V	I_{OL} = 1.6mA[1)]
Output high voltage (port 0, ALE, PSEN)	$V_{OL\ 1}$	-	0.45	V	I_{OL} = 3.2mA[1)]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	- -	V	I_{OH} = - 80 §Ë I_{OH} = - 10 §Ë
Output high voltage (port 0 in external bus mode, ALE, PSEN)	$V_{OH\ 1}$	2.4 0.9V_{CC}	- -	V	I_{OH} = - 800 §Ë[2)] I_{OH} = - 80 §Ë[2)]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	§Ë	V_{IN} = 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	§Ë	V_{IN} = 2V
Input leakage current (port 0, EA)	I_{LI}	-	±1	§Ë	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	-	10	pF	f_C = 1MHz T_A = 25 ¡É
Power supply current: Active mode, 12MHz [6)] Idle mode, 12MHz [6)] Active mode, 24 MHz [6)] Idle mode, 24MHz [6)] Active mode, 33 MHz [6)] Idle mode, 33 MHz [6)] Active mode, 40 MHz [6)] Idle mode, 40 MHz [6)] Power Down Mode	 I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{PD}	 - - - - - - - - -	 21 4.8 36.2 8.2 45 10 56.5 12.5 50	 mA mA mA mA mA mA mA mA §Ë	 V_{CC} = 5V [4)] V_{CC} = 5V [5)] V_{CC} = 5V [4)] V_{CC} = 5V [5)] V_{CC} = 5V [4)] V_{CC} = 5V [5)] V_{CC} = 5V [4)] V_{CC} = 5V [5)] V_{CC} = 5V [3)]

DC Characteristics for GMS90C54/56/58

V_{CC} = 5 V + 10%, - 15%; V_{SS} = 0 V; T_A = 0 ¡É to 70 ¡É

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except EA, RESET)	V_{IL}	-0.5	0.2 V_{CC} - 0.1	V	-
Input low voltage (EA)	$V_{IL\ 1}$	-0.5	0.2 V_{CC} - 0.3	V	-
Input low voltage (RESET)	$V_{IL\ 2}$	-0.5	0.2 V_{CC} + 0.1	V	-
Input high voltage (except XTAL1, EA, RESET)	V_{IH}	0.2V_{CC} + 0.9	V_{CC} + 0.5	V	-
Input high voltage to XTAL1	$V_{IH\ 1}$	0.7V_{CC}	V_{CC} + 0.5	V	-
Input high voltage to EA, RESET	$V_{IH\ 2}$	0.6V_{CC}	V_{CC} + 0.5	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45	V	I_{OL} = 1.6mA[1)]
Output high voltage (port 0, ALE, PSEN)	$V_{OL\ 1}$	-	0.45	V	I_{OL} = 3.2mA[1)]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	- -	V	I_{OH} = - 80 §Ë I_{OH} = - 10 §Ë
Output high voltage (port 0 in external bus mode, ALE, PSEN)	$V_{OH\ 1}$	2.4 0.9V_{CC}	- -	V	I_{OH} = - 800 §Ë[2)] I_{OH} = - 80 §Ë[2)]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	§Ë	V_{IN} = 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	§Ë	V_{IN} = 2V
Input leakage current (port 0, EA)	I_{LI}	-	±1	§Ë	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	-	10	pF	f_C = 1MHz T_A = 25 ¡É
Power supply current: Active mode, 12MHz [6)] Idle mode, 12MHz [6)] Active mode, 24 MHz [6)] Idle mode, 24MHz [6)] Active mode, 33 MHz [6)] Idle mode, 33 MHz [6)] Power Down Mode	 I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{PD}	 - - - - - - -	 TBD TBD TBD TBD TBD TBD 50	 mA mA mA mA mA mA §Ë	 V_{CC} = 5V [4)] V_{CC} = 5V [5)] V_{CC} = 5V [4)] V_{CC} = 5V [5)] V_{CC} = 5V [4)] V_{CC} = 5V [5)] V_{CC} = 5V [3)]

DC Characteristics for GMS97C51/52/54/56/58

V_{CC} = 5 V + 10%, - 15%; V_{SS} = 0 V; T_A = 0 ¡É to 70 ¡É

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except EA, RESET)	V_{IL}	-0.5	0.2 V_{CC} - 0.1	V	-
Input low voltage (EA)	$V_{IL\ 1}$	-0.5	0.1 V_{CC} - 0.1	V	-
Input low voltage (RESET)	$V_{IL\ 2}$	-0.5	0.2 V_{CC} + 0.1	V	-
Input high voltage (except XTAL1, EA, RESET)	V_{IH}	0.2V_{CC} + 0.9	V_{CC} + 0.5	V	-
Input high voltage to XTAL1	$V_{IH\ 1}$	0.7V_{CC}	V_{CC} + 0.5	V	-
Input high voltage to EA, RESET	$V_{IH\ 2}$	0.6V_{CC}	V_{CC} + 0.5	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45	V	I_{OL} = 1.6mA[1)]
Output high voltage (port 0, ALE, PSEN)	$V_{OL\ 1}$	-	0.45	V	I_{OL} = 3.2mA[1)]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	- -	V	I_{OH} = - 80 §Ë I_{OH} = - 10 §Ë
Output high voltage (port 0 in external bus mode, ALE, PSEN)	$V_{OH\ 1}$	2.4 0.9V_{CC}	- -	V	I_{OH} = - 800 §Ë[2)] I_{OH} = - 80 §Ë[2)]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	§Ë	V_{IN} = 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	§Ë	V_{IN} = 2V
Input leakage current (port 0, EA)	I_{LI}	-	±1	§Ë	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	-	10	pF	f_C = 1MHz T_A = 25 ¡É
Power supply current: Active mode, 12 MHz [6)] Idle mode, 12 MHz [6)] Active mode, 24 MHz [6)] Idle mode, 24 MHz [6)] Active mode, 33 MHz [6)] Idle mode, 33 MHz [6)] Power down mode	 I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{PD}	 - - - - - - -	 21 18 36 20 47 25 50	 mA mA mA mA mA mA §Ë	 V_{CC} = 5V [4)] V_{CC} = 5V [5)] V_{CC} = 5V [4)] V_{CC} = 5V [5)] V_{CC} = 5V [4)] V_{CC} = 5V [5)] V_{CC} = 5V [3)]

DC Characteristics for GMS90L31/32, GMS90L51/52,
GMS90L31B/32B, GMS90L51B/52B (Low voltage version)

V_{CC} = 3.3 V + 0.3V, - 0.6V; V_{SS} = 0 V; T_A = 0 ~ 70 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage	V_{IL}	-0.5	0.8	V	-
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	-
Output low voltage Port 1,2,3 Port 0,EA,RESET Port 1,2,3 Port 0,EA,RESET	 $V_{OL\,1}$ $V_{OL\,2}$ $V_{OL\,3}$ $V_{OL\,4}$	 - - - -	 0.45 0.45 0.3 0.3	 V V V V	 I_{OL} = 1.6mA [1] I_{OL} = 3.2mA [1] I_{OL} = 100μA [1] I_{OL} = 200μA [1]
Output high voltage Port 1,2,3 Port 0 in external bus mode, ALE,PSEN	 $V_{OH\,1}$ $V_{OH\,2}$ $V_{OH\,3}$ $V_{OH\,4}$	 2.0 0.9V_{CC} 2.0 0.9V_{CC}	 - - - -	 V V V V	 I_{OH} = -20μA I_{OH} = -10μA I_{OH} = -800μA [2] I_{OH} = -80μA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-1	-50	μA	V_{IN} = 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-25	-250	μA	V_{IN} = 2.0V
Input leakage current (port 0, EA)	I_{LI}	-	±1	μA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	-	10	pF	f_C = 1MHz T_A = 25 °C
Power supply current: Active mode, 12 MHz Idle mode, 12 MHz Power Down Mode	 I_{CC} I_{CC} I_{PD}	 - - -	 11 5 15	 mA mA μA	 V_{CC} = 3.6V [4] V_{CC} = 3.6V [5] V_{CC} = 2 ... 3.6V [3]

DC Characteristics for GMS90L54/56/58 (Low voltage version)

V_{CC} = 3.3 V + 0.3V, - 0.6V; V_{SS} = 0 V; T_A = 0 ~ 70 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage	V_{IL}	-0.5	0.8	V	-
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	-
Output low voltage Port 1,2,3 Port 0,EA,RESET Port 1,2,3 Port 0,EA,RESET	 $V_{OL\,1}$ $V_{OL\,2}$ $V_{OL\,3}$ $V_{OL\,4}$	 - - - -	 0.45 0.45 0.3 0.3	 V V V V	 I_{OL} = 1.6mA [1] I_{OL} = 3.2mA [1] I_{OL} = 100µA [1] I_{OL} = 200µA [1]
Output high voltage Port 1,2,3 Port 0 in external bus mode, ALE,PSEN	 $V_{OH\,1}$ $V_{OH\,2}$ $V_{OH\,3}$ $V_{OH\,4}$	 2.0 0.9V_{CC} 2.0 0.9V_{CC}	 - - - -	 V V V V	 I_{OH} = -20µA I_{OH} = -10µA I_{OH} = -800µA [2] I_{OH} = -80µA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-1	-50	µA	V_{IN} = 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-25	-250	µA	V_{IN} = 2.0V
Input leakage current (port 0, EA)	I_{LI}	-	±1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	-	10	pF	f_C = 1MHz T_A = 25 °C
Power supply current: Active mode, 12 MHz Idle mode, 12 MHz Power Down Mode	 I_{CC} I_{CC} I_{PD}	 - - -	 TBD TBD TBD	 mA mA µA	 V_{CC} = 3.6V [4] V_{CC} = 3.6V [5] V_{CC} = 2 ... 3.6V [3]

DC Characteristics for GMS97L51/52/54/56/58 (Low voltage version)

V_{CC} = 3.3 V + 0.3V, - 0.6V; V_{SS} = 0 V; T_A = 0 ¡É to 70 ¡É

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage	V_{IL}	-0.5	0.8	V	-
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	-
Output low voltage Port 1,2,3 Port 0,EA,RESET Port 1,2,3 Port 0,EA,RESET	 $V_{OL\,1}$ $V_{OL\,2}$ $V_{OL\,3}$ $V_{OL\,4}$	 - - - -	 0.45 0.45 0.3 0.3	 V V V V	 I_{OL} = 1.6mA [1] I_{OL} = 3.2mA [1] I_{OL} = 100§Ë [1] I_{OL} = 200§Ë [1]
Output high voltage Port 1,2,3 Port 0 in external bus mode, ALE,PSEN	 $V_{OH\,1}$ $V_{OH\,2}$ $V_{OH\,3}$ $V_{OH\,4}$	 2.0 0.9V_{CC} 2.0 0.9V_{CC}	 - - - -	 V V V V	 I_{OH} = -20§Ë I_{OH} = -10§Ë I_{OH} = -800§Ë [2] I_{OH} = -80§Ë [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-1	-50	§Ë	V_{IN} = 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-25	-250	§Ë	V_{IN} = 2.0V
Input leakage current (port 0, EA)	I_{LI}	-	±1	§Ë	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	-	10	pF	f_C = 1MHz T_A = 25¡É
Power supply current: Active mode, 12 MHz Idle mode, 12 MHz Power Down Mode	 I_{CC} I_{CC} I_{PD}	 - - -	 11 5 15	 mA mA §Ë	 V_{CC} = 3.6V [4] V_{CC} = 3.6V [5] V_{CC} = 3.6V [3]

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading: > 50pF at 3.3V, > 100pF at 5V), the noise pulse on ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $0.9V_{CC}$ specification when the address lines are stabilizing.

3) I_{PD} (Power Down Mode) is measured under following conditions:
EA = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} - 0.5V; XTAL2 = N.C.;
EA = Port0 = RESET = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} - 0.5V; XTAL2 = N.C.;
RESET = EA = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

6) $I_{CC\ max}$ at other frequencies is given by:
active mode: I_{CC} = 1.27 ¡¿ f_{OSC} + 5.73
idle mode: I_{CC} = 0.28 ¡¿ f_{OSC} + 1.45 (except OTP devices)
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5V.

AC Characteristics for GMS90 series (12MHz version)

Vcc = 5 V *:* V_{CC} = 5 V + 10%, -15%; V_{SS} = 0 V; TA = 0°C to 70°C
(C_L for port 0. ALE and PSEN outputs = 100pF; CL for all other outputs = 80 pF)

Vcc = 3.3 V *:* V_{CC} = 3.3 V + 0.3 V, -0.6 V; V_{SS} = 0 V; TA = 0°C to 70°C
(C_L for port 0. ALE and $\overline{\text{PSEN}}$ outputs = 50pF; C_L for all other outputs = 50 pF)

Variable clock : Vcc = 5V : $1/t_{CLCL}$ = 3.5 MHz to 12 MHz
Vcc = 3.3V : $1/t_{CLCL}$ = 1 MHz to 12 MHz

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	-	$2t_{CLCL}$ - 40	-	ns
Address setup to ALE	t_{AVLL}	43	-	t_{CLCL} - 40	-	ns
Address hold after ALE	t_{LLAX}	30	-	t_{CLCL} -53	-	ns
ALE low to valid instr in	t_{LLIV}	-	233	-	$4t_{CLCL}$ - 100	ns
ALE to PSEN	t_{LLPL}	58	-	t_{CLCL} - 25	-	ns
PSEN pulse width	t_{PLPH}	215	-	$3t_{CLCL}$ - 35	-	ns
PSEN to valid instr in	t_{PLIV}	-	150	-	$3t_{CLCL}$ - 100	ns
Input instruction hold after PSEN	t_{PXOX}	0	-	0	-	ns
Input instruction float after PSEN	t_{PXIZ} *)	-	63	-	t_{CLCL} - 20	ns
Address valid after PSEN	t_{PXAV} *)	75	-	t_{CLCL} - 8	-	ns
Address to valid instruction in	t_{AVIV}	-	302	-	$5t_{CLCL}$ - 115	ns
Address float to PSEN	t_{AZPL}	0	-	0	-	ns

*) Interfacing the GMS90 series to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for GMS90 series (12MHz version)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock		
		min.	max.	min.	max.	
RD pulse width	t_{RLRH}	400	-	$6t_{CLCL}$ - 100	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	-	$6t_{CLCL}$ - 100	-	ns
Address hold after ALE	t_{LLAX2}	53	-	t_{CLCL} - 30	-	ns
RD to valid data in	t_{RLDV}	-	252	-	$5t_{CLCL}$ - 165	ns
Data hold after RD	t_{RHDX}	0	-	0	-	ns
Data float after RD	t_{RHDZ}	-	97	-	$2t_{CLCL}$ - 70	ns
ALE to valid data in	t_{LLDV}	-	517	-	$8t_{CLCL}$ - 150	ns
Address to valid data in	t_{AVDV}	-	585	-	$9t_{CLCL}$ - 165	ns
ALE to $\overline{WR}$ or RD	t_{LLWL}	200	300	$3t_{CLCL}$ - 50	$3t_{CLCL}$ +50	ns
Address valid to $\overline{WR}$ or RD	t_{AVWL}	203	-	$4t_{CLCL}$ - 130	-	ns
$\overline{WR}$ or RD high to ALE high	t_{WHLH}	43	123	t_{CLCL} - 40	t_{CLCL} +40	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	-	t_{CLCL} - 50	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	-	$7t_{CLCL}$ - 150	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	-	t_{CLCL} - 50	-	ns
Address float after RD	t_{RLAZ}	-	0	-	0	ns

Advance Information (12MHz version)

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable clock		
		min.	max.	
Oscillator period(Vcc=5V) Oscillator period(Vcc=3.3V)	t_{CLCL} t_{CLCL}	83.3 83.3	285.7 1	ns us
High time	t_{CHCX}	20	t_{CLCL} - t_{CLCX}	ns
Low time	t_{CLCX}	20	t_{CLCL} - t_{CHCX}	ns
Rise time	t_{CLCH}	-	20	ns
Fall time	t_{CHCL}	-	20	ns

AC Characteristics for GMS90 series (24MHz version)

V_{CC} = 5 V + 10%, - 15%; V_{SS} = 0 V; T_A = 0°C to 70°C

(C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	43	-	$2t_{CLCL}$ - 40	-	ns
Address setup to ALE	t_{AVLL}	17	-	t_{CLCL} - 25	-	ns
Address hold after ALE	t_{LLAX}	17	-	t_{CLCL} - 25	-	ns
ALE low to valid instr in	t_{LLIV}	-	80	-	$4t_{CLCL}$ - 87	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	22	-	t_{CLCL} - 20	-	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	95	-	$3t_{CLCL}$ - 30	-	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	-	60	-	$3t_{CLCL}$ - 65	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	-	32	-	t_{CLCL} - 10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	37	-	t_{CLCL} - 5	-	ns
Address to valid instruction in	t_{AVIV}	-	148	-	$5t_{CLCL}$ - 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	-	0	-	ns

*) Interfacing the GMS90 series to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC characteristics for GMS90 series (24MHz version)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	180	-	$6t_{CLCL}$ - 70	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	180	-	$6t_{CLCL}$ - 70	-	ns
Address hold after ALE	t_{LLAX2}	15	-	t_{CLCL} - 27	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	118	-	$5t_{CLCL}$ - 90	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	63	-	$2t_{CLCL}$ - 20	ns
ALE to valid data in	t_{LLDV}	-	200	-	$8t_{CLCL}$ - 133	ns
Address to valid data in	t_{AVDV}	-	220	-	$9t_{CLCL}$ - 155	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	75	175	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	67	-	$4t_{CLCL}$ - 97	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	17	67	t_{CLCL} - 25	t_{CLCL} + 25	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	-	t_{CLCL} - 37	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	170	-	$7t_{CLCL}$ - 122	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	15	-	t_{CLCL} - 27	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

Advance Information (24MHz version)

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable clock Freq. = 3.5 MHz to 24 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	41.7	285.7	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	-	12	ns
Fall time	t_{CHCL}	-	12	ns

AC Characteristics for GMS90 series (33MHz version)

V_{CC} = 5 V + 10%, -15%; V_{SS} = 0 V; T_A = 0 °C to 70 °C

(C_L for port 0, ALE and PSEN outputs = 100pF; C_L for all other outputs =80pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		33 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 33 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	40	-	$2t_{CLCL}$ - 20	-	ns
Address setup to ALE	t_{AVLL}	10	-	t_{CLCL} - 20	-	ns
Address hold after ALE	t_{LLAX}	10	-	t_{CLCL} - 20	-	ns
ALE low to valid instr in	t_{LLIV}	-	56	-	$4t_{CLCL}$ - 65	ns
ALE to $\overline{PSEN}$	t_{LLPL}	15	-	t_{CLCL} - 15	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	80	-	$3t_{CLCL}$ - 20	-	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	-	35	-	$3t_{CLCL}$ - 55	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	-	20	-	t_{CLCL} - 10	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	25	-	t_{CLCL} - 5	-	ns
Address to valid instruction in	t_{AVIV}	-	91	-	$5t_{CLCL}$ - 60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	-	0	-	ns

*) Interfacing the GMS90 series to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for GMS90series (33MHz version)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		33 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 33 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	132	-	$6t_{CLCL}$ - 50	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	132	-	$6t_{CLCL}$ - 50	-	ns
Address hold after ALE	t_{LLAX2}	10	-	t_{CLCL} - 20	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	81	-	$5t_{CLCL}$ - 70	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	46	-	$2t_{CLCL}$ - 15	ns
ALE to valid data in	t_{LLDV}	-	153	-	$8t_{CLCL}$ - 90	ns
Address to valid data in	t_{AVDV}	-	183	-	$9t_{CLCL}$ - 90	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	71	111	$3t_{CLCL}$ - 20	$3t_{CLCL}$ + 20	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	66	-	$4t_{CLCL}$ - 55	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	t_{CLCL} - 20	t_{CLCL} + 20	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	-	t_{CLCL} - 25	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	142	-	$7t_{CLCL}$ - 70	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	10	-	t_{CLCL} - 20	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

Advance Information (33MHz version)

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable clock Freq. = 3.5 MHz to 33 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	30.3	285.7	ns
High time	t_{CHCX}	11.5	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	11.5	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	-	5	ns
Fall time	t_{CHCL}	-	5	ns

AC Characteristics for GMS90 series (40MHz version)

V_{CC} = 5 V + 10%, -15%; V_{SS} = 0 V; T_A = 0 °C to 70 °C
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all other outputs =80pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	-	$2t_{CLCL}$ - 15	-	ns
Address setup to ALE	t_{AVLL}	10	-	t_{CLCL} - 15	-	ns
Address hold after ALE	t_{LLAX}	10	-	t_{CLCL} - 15	-	ns
ALE low to valid instr in	t_{LLIV}	-	55	-	$4t_{CLCL}$ - 45	ns
ALE to $\overline{PSEN}$	t_{LLPL}	10	-	t_{CLCL} - 15	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	60	-	$3t_{CLCL}$ - 15	-	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	-	25	-	$3t_{CLCL}$ - 50	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	-	15	-	t_{CLCL} - 10	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	20	-	t_{CLCL} - 5	-	ns
Address to valid instruction in	t_{AVIV}	-	65	-	$5t_{CLCL}$ - 60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	-50	-	- 5	-	ns

*) Interfacing the GMS90 series to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for GMS90series (40MHz version)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	-	$6t_{CLCL}$ - 30	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	-	$6t_{CLCL}$ - 30	-	ns
Address hold after ALE	t_{LLAX2}	10	-	t_{CLCL} - 15	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	75	-	$5t_{CLCL}$ - 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	38	-	$2t_{CLCL}$ - 12	ns
ALE to valid data in	t_{LLDV}	-	150	-	$8t_{CLCL}$ - 50	ns
Address to valid data in	t_{AVDV}	-	150	-	$9t_{CLCL}$ - 75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	$3t_{CLCL}$ - 15	$3t_{CLCL}$ + 15	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	-	$4t_{CLCL}$ - 30	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	t_{CLCL} - 15	t_{CLCL} + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	-	t_{CLCL} - 20	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	-	$7t_{CLCL}$ - 50	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	-	t_{CLCL} - 20	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

Advance Information (40MHz version)

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	25	285.7	ns
High time	t_{CHCX}	10	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	10	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	-	10	ns
Fall time	t_{CHCL}	-	10	ns

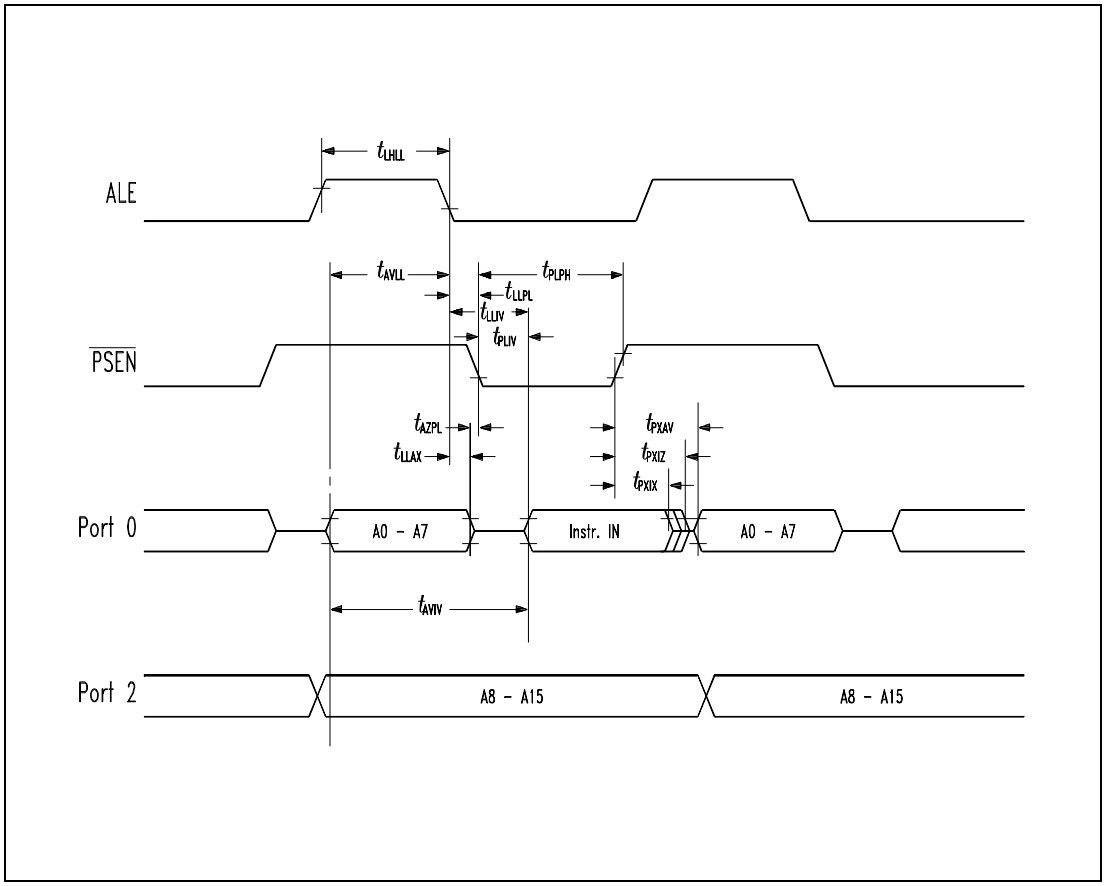


Figure 4
Program Memory Read Cycle

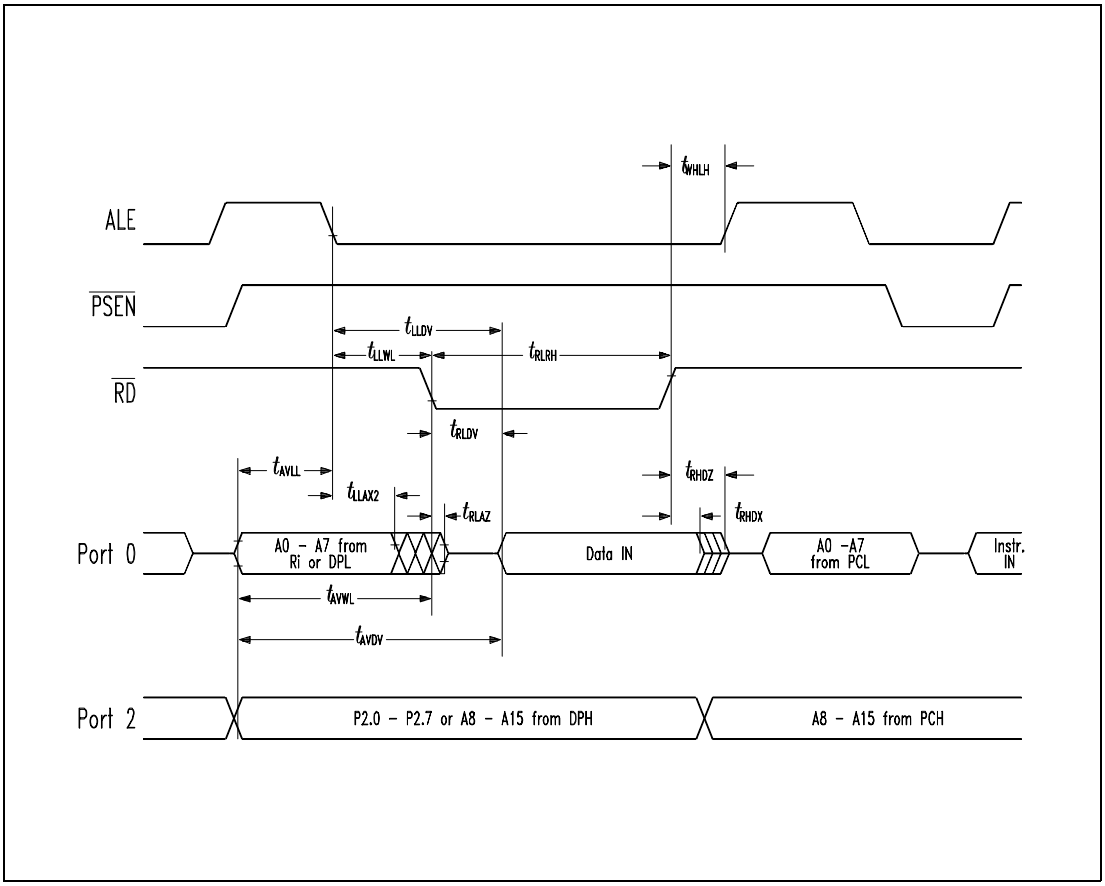


Figure 5
Data Memory Read Cycle

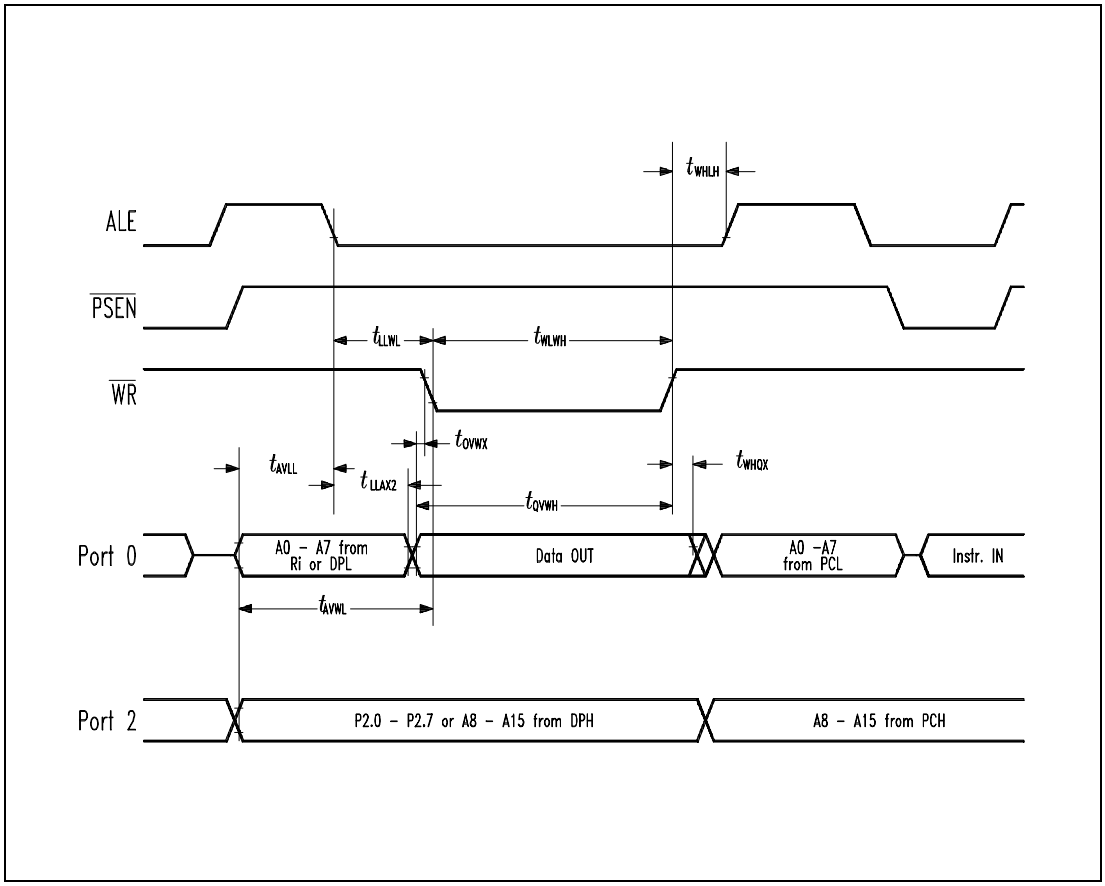
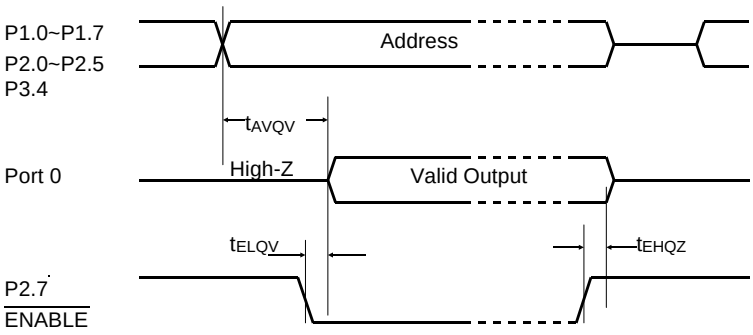


Figure 6
Data Memory Write Cycle

OTP ROM Verification Characteristics

ROM Verification Mode 1

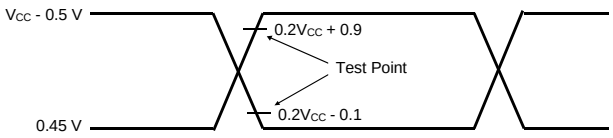
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	-	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	-	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0 - P1.7 = A0 - A7
P2.0 - P2.5 = A8 - A13
P3.4 = A14
Data: P0.0 - P0.7 = D0 - D7

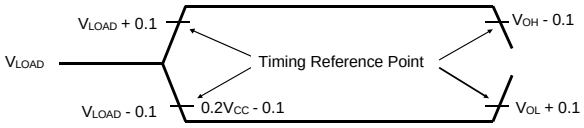
Inputs: P2.6, $\overline{PSEN}=V_{SS}$
ALE, $\overline{EA} = V_{IH}$
RESET = V_{IH1}

Figure 7
OTP ROM Verification Mode 1



AC Inputs during testing are driven at V_{CC} - 0.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at V_{IHmin} for a logic "1" and V_{ILmax} for a logic "0".

Figure 8
AC Testing : Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100mV change from load voltage occurs and begins to float when a 100mV change from the loaded V_{OH} / V_{OL} level occurs.
I_{OL} / I_{OH} ¡Ã 20mA.

Figure 9
AC Testing : Float Waveforms

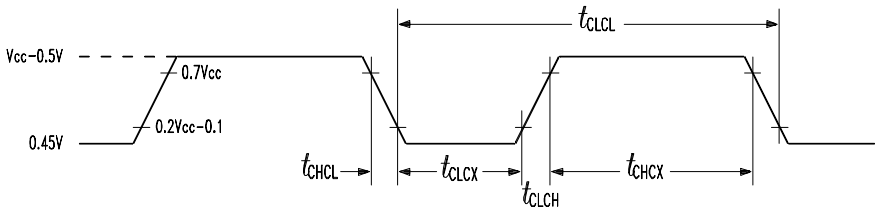


Figure 10
External Clock Cycle

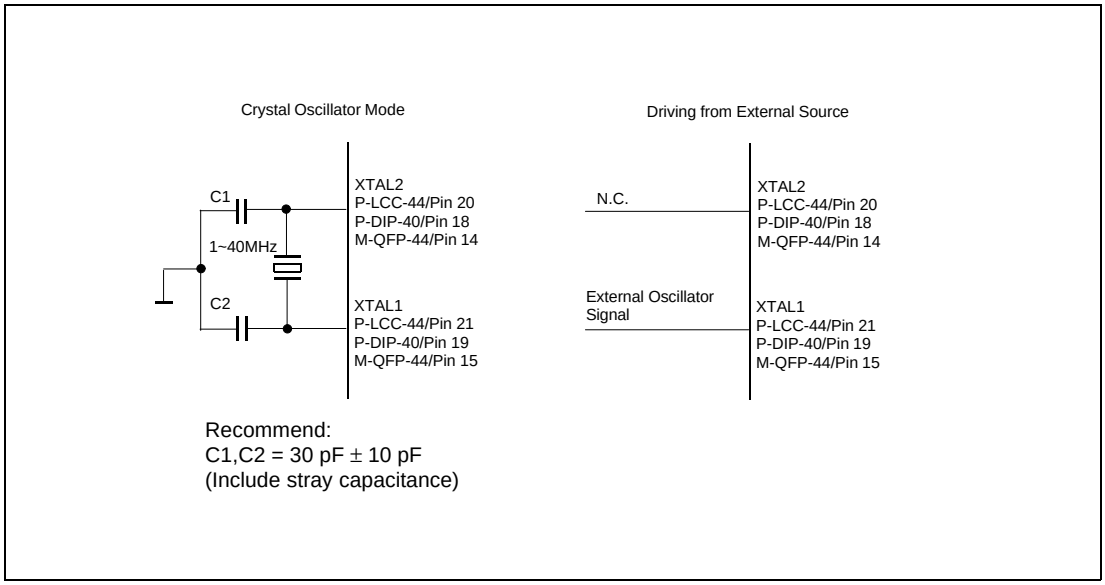


Figure 11
Recommended Oscillator Circuits

EPROM Characteristics

The GMS97C5x, 97L5x are programmed by using a modified Quick-Pulse Programming^{TM} algorithm. It differs from older methods in the value used for Vpp (programming supply voltage) and in the width and number of the ALE/PROG pulses. The GMS97C5x, 97L5x contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an manufactured by LGS. Table 11 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 12 and 13. Figure 14 shows the circuit configuration for normal program memory verification.

Quick-pulse programming

The setup for microcontroller quick-pulse programming is shown in Figure 13. Note that the GMS97C5x, 97L5x is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers. The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 12. The code byte to be programmed into that location is applied to port 0, RST, PSEN and pins of port 2 and 3 in Table 11 are held at the "Program Data" levels indicated in Table 11. The ALE/PROG is pulsed low 25 times as shown Figure 13. To program the encryption table, repeat the 25 pulses (10 pulses for 97x54/56/58) programming sequence for addresses 0 through $1F_H$($3F_H$ for 97x54/56/58), using the "Pgm Encryption Table" levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data. To program the security bits, repeat the 25 pulses (10 pulses for 97x54/56/58) programming sequence using the "Pgm Security Bit" levels after one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed. Note that the EA/V_{PP} pin must not be allowed to go above the maximum specified Vpp level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free glitches and overshoot.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory location to be read is applied to ports 1 and 2 as shown in Figure 15. The other pins are held at the "Verify Code Data" levels indicated in Table 11. The contents of the address location will be emitted on port 0 for this operation. If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Program Memory Lock Bits

The two-level Program Lock system consists of 2 Lock bits and a 32-byte (64-byte for GMS97x54/56/58) Encryption Array which are used to protect the program memory against software piracy.

Encryption Array:

Within the EPROM array are 32 bytes (64 bytes for GMS97x54/56/58) of Encryption Array that are initially unprogrammed (all 1s). Every time that a byte is addressed during a verify, address lines are used to select a byte of the Encryption array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an Encrypted Verify byte.

The algorithm, with the array in the unprogrammed state (all 1s), will return the code in its original, unmodified form, It is recommended that whenever the Encryption Array is used, at least one of the Lock Bits be programmed as well.

Lock Bit Protection Modes

Program Lock Bits			Protection Type
	LB1	LB2	
1	U	U	No program lock features
2	P	U	Futher programming of the EPROM is disabled
3	P	P	Same as mode 2, also verify is disabled

U: unprogrammed, P: programmed

Reading the Signature Bytes :

The GMS97x51/52 signature bytes in locations 030_H and 031_H, the GMS97x54/56/58 signature bytes in locations 030_H and 060_H. To read these bytes follow the procedure for EPROM verify, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

Location	Device	Contents
30H	All	E0H
31H	GMS97C51/L51	73H
	GMS97C52/L52	71H
60H	GMS97C54/L54	54H
	GMS97C56/L56	56H
	GMS97C58/L58	58H

Program / Verify algorithms

Any algorithm in agreement with the conditions listed in Table 11, and which satisfies the timing specifications is suitable.

Table 11. EPROM programming modes

MODE	RST	PSEN	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.7	P2.6	P3.7	P3.6
Read Signature	1	0	1	1	0	0	0	0
Program Code Data	1	0	0	V_{PP}	1	0	1	1
Verify Code Data	1	0	1	1	0	0	1	1
Program encryption table	1	0	0	V_{PP}	1	0	1	0
Program security bit 1	1	0	0	V_{PP}	1	1	1	1
Program security bit 2	1	0	0	V_{PP}	1	1	0	0

Notes :
1. "0" = Valid low for that pin, "1" = valid high for that pin.
2. Vpp = 12.75V ± 0.25V
3. Vcc = 5V ± 10% during programming and verification.
4. ALE/$\overline{PROG}$ receives 25 (10 for GMS97x54/56/58) programming pulses while V_{PP} is held at 12.75. Each programming pulse is low for 100us (± 10us) and high for a minimum of 10us.

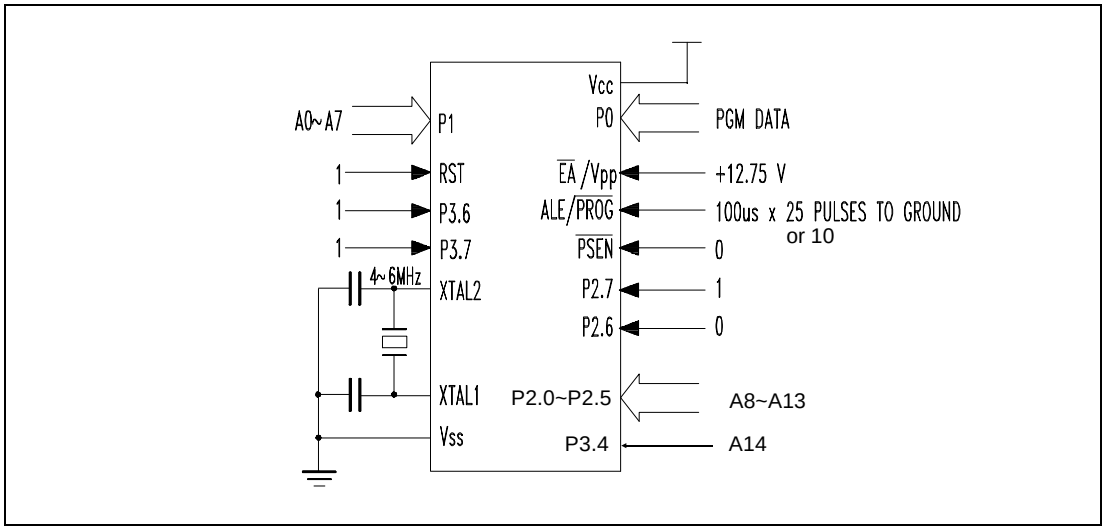


Figure 12
Programming Configuration

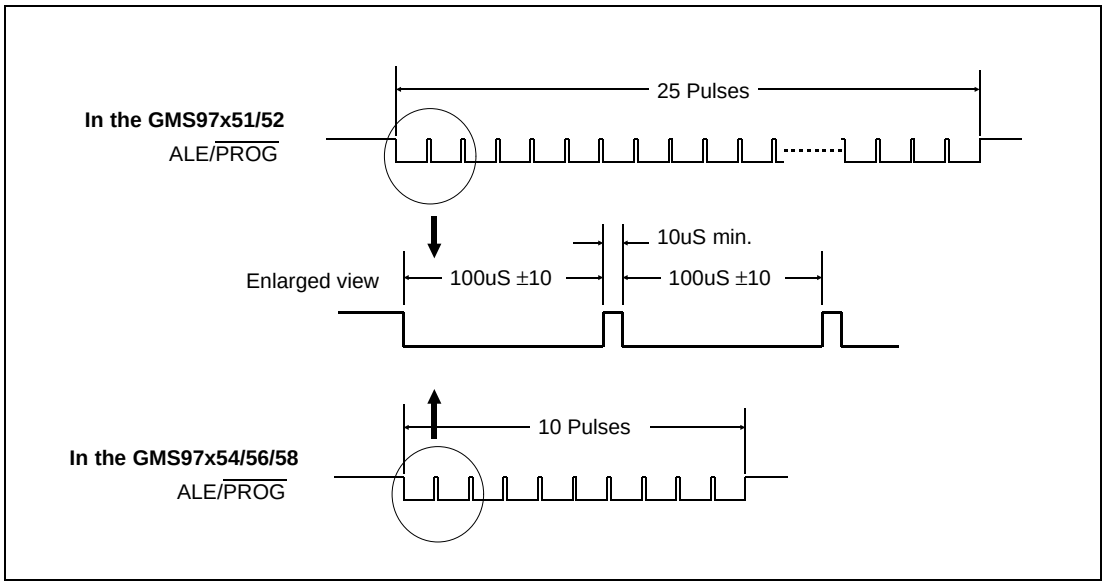


Figure 13
PROG Waveform

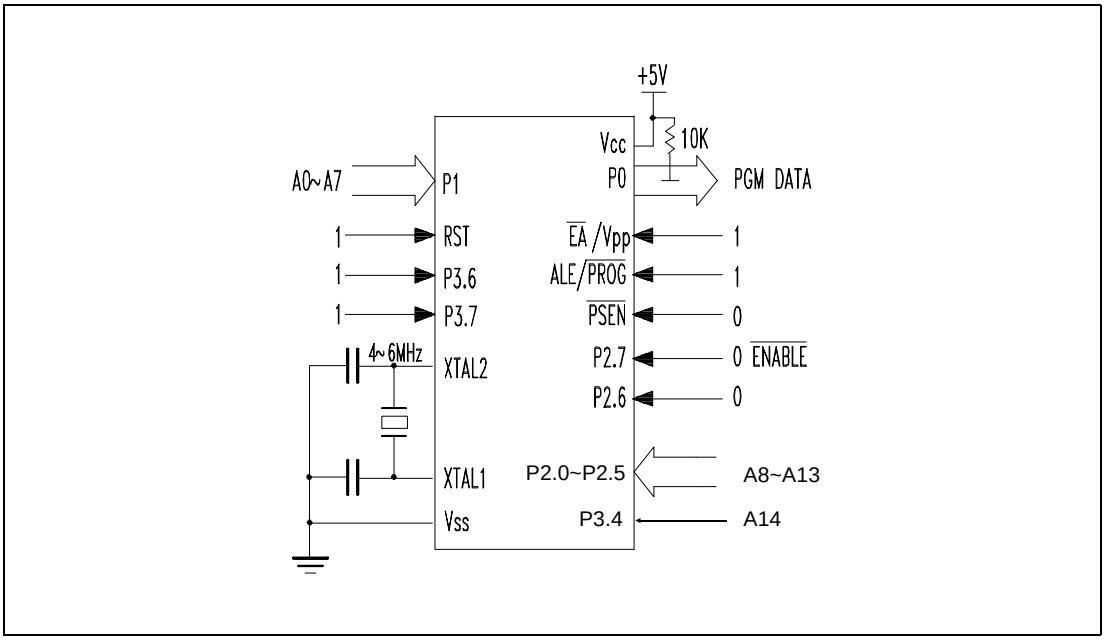
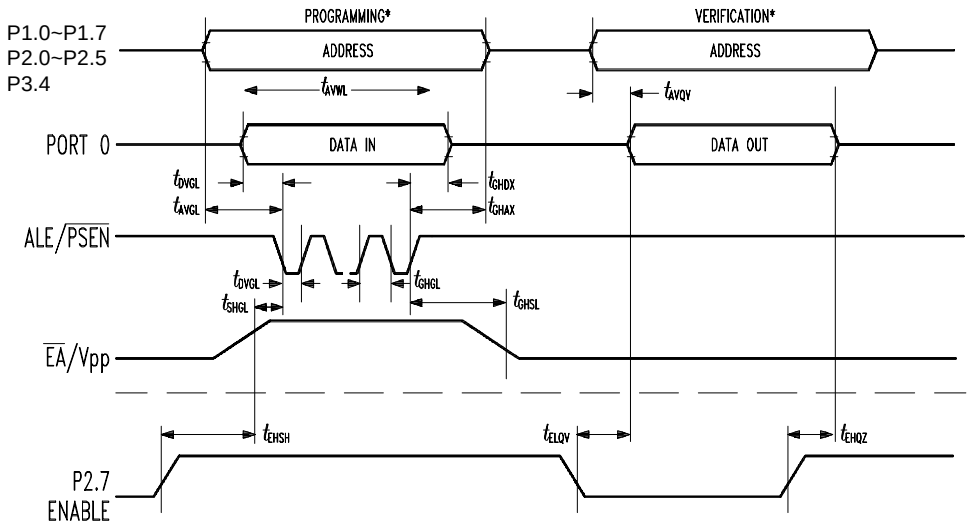


Figure 14
Program Verification

EPROM Programming and Verification Characteristics
T_A = 21¡É to 27¡É Vcc = 5V ± 10%, Vss = 0V (See Figure 15)

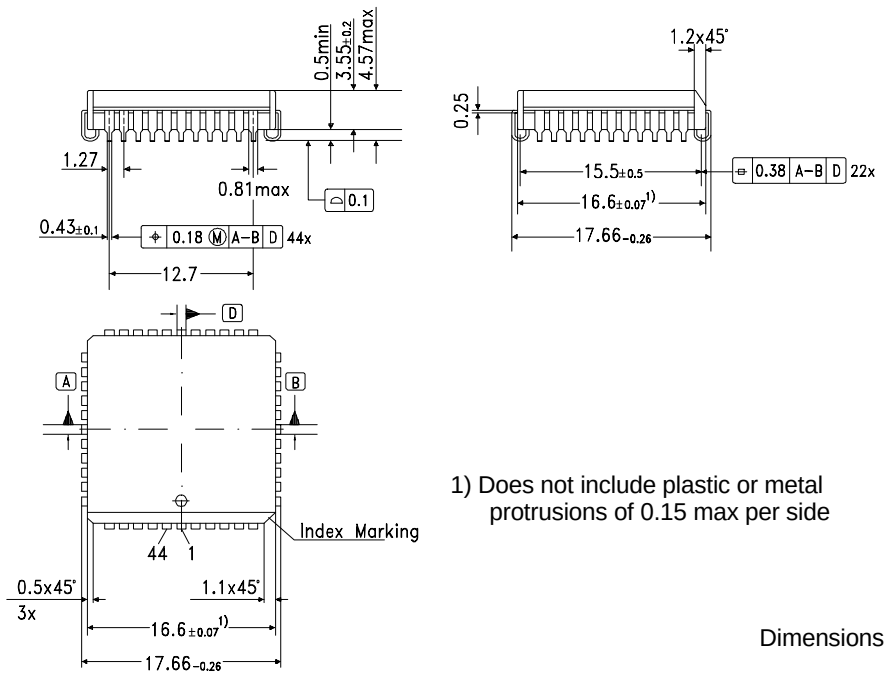
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Programming supply voltage	V_{PP}	12.5	13.0	V
Programming supply current	I_{PP}	-	50	mA
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz
Address setup to PROG low	t_{AVGL}	$48t_{CLCL}$	-	-
Address hold after PROG	t_{GHAX}	$48t_{CLCL}$	-	-
Data setup to PROG low	t_{DVGL}	$48t_{CLCL}$	-	-
Data setup after PROG	t_{GHDX}	$48t_{CLCL}$	-	-
P2.7 (ENABLE) high to V_{PP}	t_{EHSH}	$48t_{CLCL}$	-	-
V_{PP} setup to PROG low	t_{SHGL}	10	-	us
V_{PP} hold after PROG	t_{GHSL}	10	-	us
PROG width	t_{GLGL}	90	110	us
Address to data valid	t_{AVQL}	-	$48t_{CLCL}$	-
ENABLE low to data valid	t_{ELQZ}	-	$48t_{CLCL}$	-
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	-
PROG high to PROG low	t_{GHGL}	10		us



For programming verification see Figure 12.
For verification conditions see Figure 14.

Figure 15
EPROM Programming and Verification

Plastic Package, P-LCC-44-SMD (Plastic Leaded Chip-Carrier)



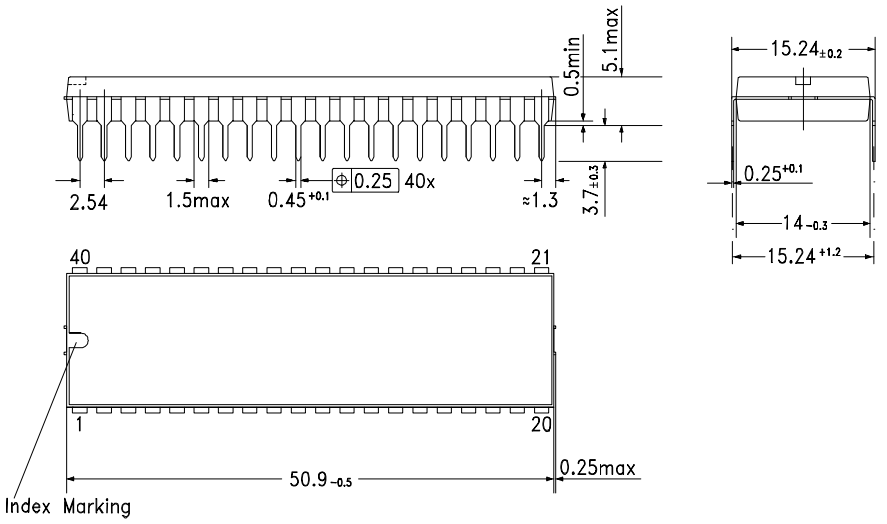
1) Does not include plastic or metal protrusions of 0.15 max per side

Dimensions in mm

SMD = Surface Mounted Device

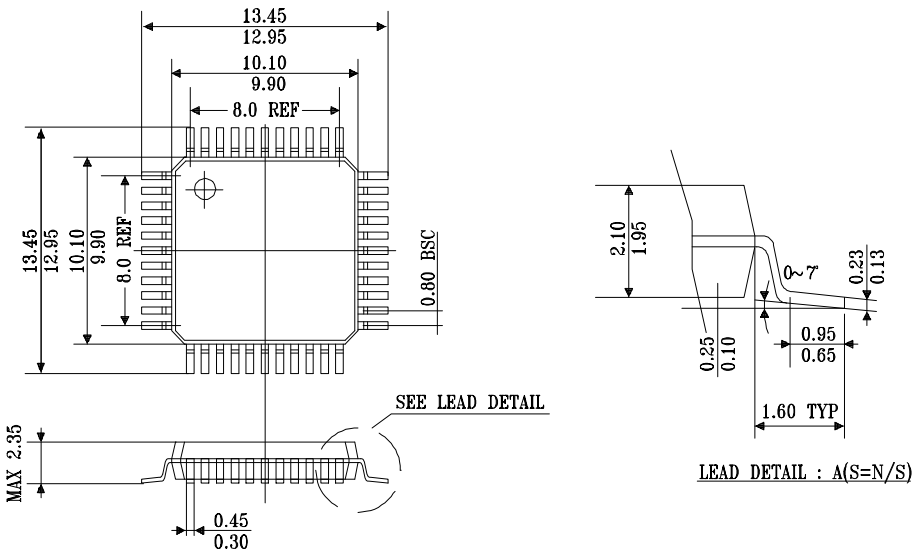
SMD = Surface Mounted Device

Plastic Package, P-DIP-40
(Plastic Dual in-Line Package)



Dimensions in mm

Plastic Package, P-MQFP-44(SMD)
(Plastic Metric Quad Flat Package)



* Does not include plastic or metal protrusions of 0.25 max per side

Dimensions in mm